TELEDYNE PHILBRICK PRODUCT GUIDE

LINEAR

DATA CONVERSION

NONLINEAR

POWER SUPPLIES

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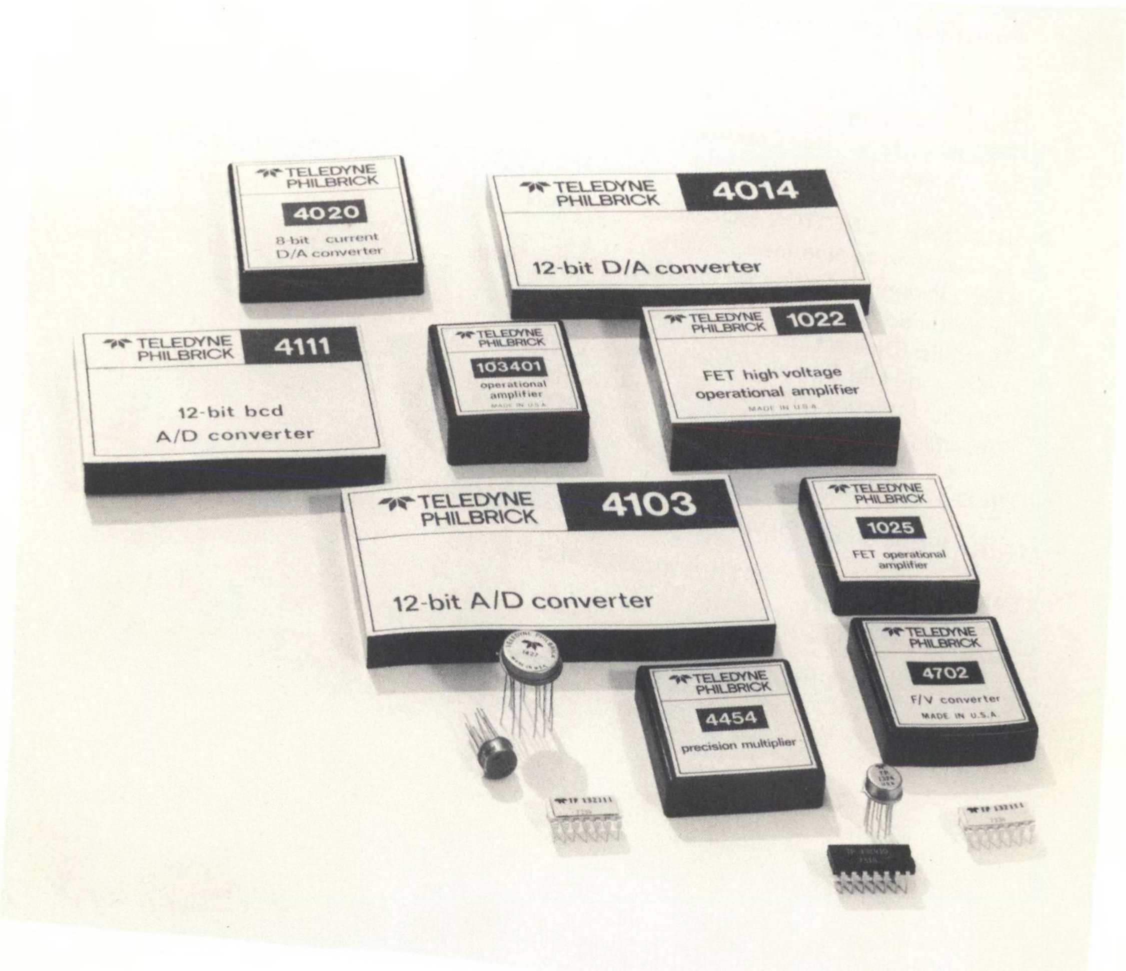
TELEDYNE PHILBRICK IS

. . . a perennial pioneer, having invented a good many of the analog techniques that are now in universal use. Since our founding in 1946 as George A. Philbrick Researches, Inc., we have been continually challenged by a few (competent) compet tors and many (imitative) latecomers, but have been able to find renewed strength in the depth of our creative resources. Fortunately that creativity, stimulated by our passionate need to lead, has kept us in the forefront of the industry.

Among the earliest Philbrick products was a series of operational amplifiers which stirred the imagination of the electronics world and pointed the way to the "packaged circuit module" design concept. From the first tube-type amplifiers produced by the company has grown an astonishing proliferation of complex and sophisticated modules encompassing a wide variety of analog and digital circuit functions including the following noteworthy firsts:

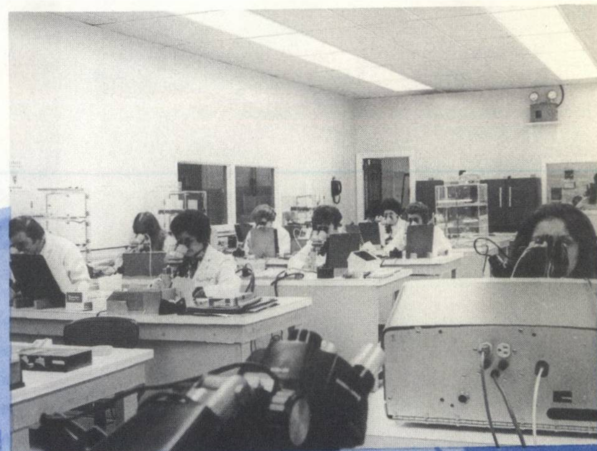
- First commercially available op amps.
- First low bias current parametric op amp (patented).
- First hermetically-sealed hybrid chopper stabilized op amp.
- First gated operational amplifier module.
- First temperature compensated log amplifier (patented).
- First low cost, high accuracy Voltage-to-Frequency (V/F) and Frequency-to-Voltage (F/V) Converters.
- First high-performance "Deglitched" D/A Converter.



TOTAL CAPABILITY... the key to success

Teledyne Philbrick's engineering, marketing, and manufacturing operations are located in a modern facility just off Route 128 . . . greater Boston's famous "Electronics Row." Operations include manufacturing facilities for discrete component products as well as thin and thick-film hybrid devices. Our facilities have been carefully designed for optimized high quality/high volume production. All manufacturing operations are constantly monitored by our quality control and engineering departments to ensure strict conformity to performance and reliability criteria . . . traditional hallmarks of the Teledyne Philbrick product line.

Throughout Teledyne Philbrick's impressive history, our foremost consideration has been the needs of our customers. Our engineers and scientists are continually pushing state-of-the-art technologies to their practical limits in order to produce products which give complete customer satisfaction, particularly relying on guaranteed performance and ease of application. All Teledyne Philbrick resources (engineering, manufacturing, quality control and marketing) are dedicated to successfully achieving this goal.



ENGINEERING...the first essential

A competent, professional, goal-oriented team of engineer-scientists working in a creatively stimulating environment is the foundation of Teledyne Philbrick's continuing success. Research, design, production, and application engineers are the product innovators who consistently provide practical, proven solutions to myriad problems within even the most difficult time and cost constraints.

Teledyne Philbrick **"Specials"**

No standard product line, however broad, can encompass the total spectrum of potential applications. Certain optimized electrical parameters or unusual package designs are sometimes necessary to meet inflexible customer requirements. Teledyne Philbrick engineers are experienced specialists in evaluating and satisfying unusual requirements.

Outstanding examples of recently developed Teledyne Philbrick **"specials"** include devices for pollution control, display systems, air traffic control, aircraft ignition systems, fetal heart monitoring, and process control systems.

How can these **"special"** talents and resources be put to work on your behalf? Let us quote on your requirements.

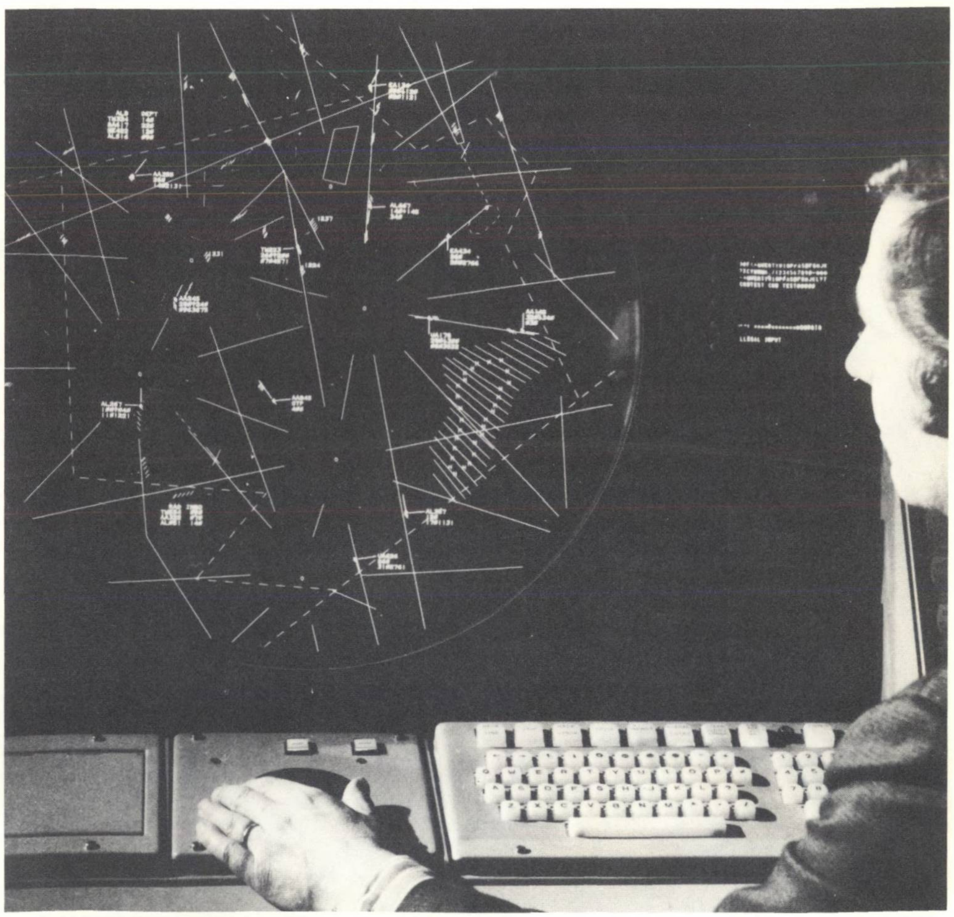


Photo courtesy of Raytheon FAA Plan View Display

MANUFACTURING...making it smaller

Teledyne Philbrick excels in the art of miniaturized packaging of high quality products. One technique extensively used to achieve this goal is hybrid packaging.

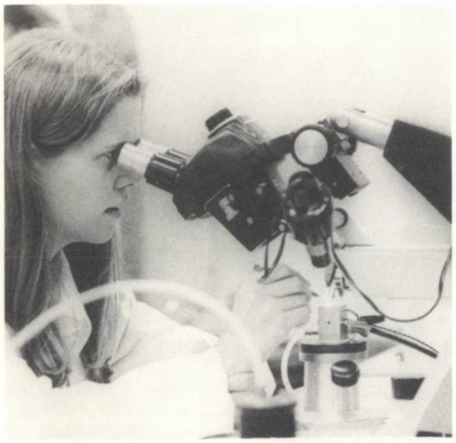
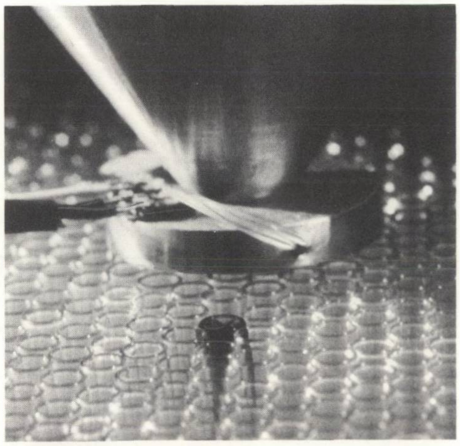
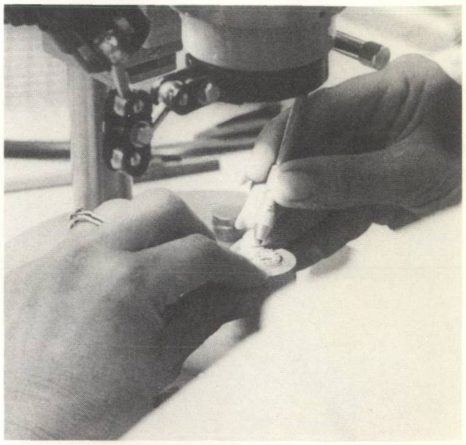
Teledyne Philbrick's manufacturing capability for the production of hybrid circuit modules is considered by many to be the finest in the industry. We have maintained our position of superiority by seeking out, developing, and implementing the most modern manufacturing methods. Our processes make maximum use of controlled automation to ensure consistent high-quality production. We are continually evaluating and evolving hybrid technologies to ensure the highest performance and reliability at the lowest possible prices.

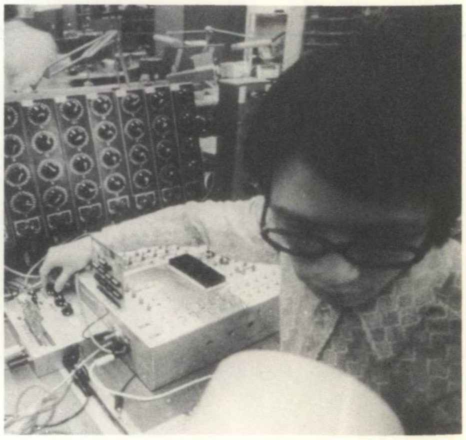
Philbrick's hybrid facility in Dedham, employs the most advanced manufacturing equipment available, some of which was solely conceived and developed at Philbrick, because our exacting technical requirements were beyond the scope of existing equipment suppliers.

One example of Philbrick's internally-designed production hardware is a computized chip tester which will test 500 transistor chips per hour and sort them into 1000 separate categories. This unique matching hardware provides us with exceptional time and cost economies and permits us to more closely control circuit performance.

Philbrick's engineering talent in advanced thick and thin-film processes is unsurpassed. Constant experimentation and accumulated years of experience have produced proprietary processing techniques that enable us to manufacture products with exceptional repeatability, reliability, and stability.

Skilled labor is a key element in the production of high quality hybrid circuits. To ensure optimum reliability and performance, quality components are assembled by proficient personnel. Their work is constantly checked by quality control inspectors who monitor every stage of production, from incoming inspection to the final appearance. All units, from the simplest to the most sophisticated, are 100% inspected electrically and mechanically.

QUALITY CONTROL... enforcing the highest standards

Teledyne Philbrick's well staffed Quality Control Department maintains the rigid standards which protect our well established reputation for products of the highest quality. Every Philbrick production lot is carefully inspected and tested at appropriate stages of the production cycle.

Military, space, and man-life equipment applications, however, require the most stringent quality-insurance guarantees. These high reliability devices are Philbrick's specialty. Military, NASA, or severe commercial qualification tests are routinely performed at Philbrick. Our products have contributed to such high-reliability projects as Apollo, Minuteman, F-4, and others.

HIGH RELIABILITY DISCRETES . . . Modular (discrete component) linear and data conversion products are manufactured in full compliance with all MIL-SPEC requirements including environmental, parts, materials, and processes with full MIL documentation. Modules have been delivered to the requirements of MIL-E-4158, MIL-E-5400, MIL-T-21200 and other specifications and are fully qualified for military system usage. MIL-STD-454 and MIL-STD-701 parts are used including JAN-TX and ER reliability-screened components with full source control and in-plant materials control. A Full Configuration Management System insures continued product uniformity, and Quality Assurance Control per MIL-Q-9858 assures complete specification conformance and product reliability.

HIGH-RELIABILITY MICROCIRCUITS

Many Philbrick Micropackaged linear and data conversion products can be processed to meet the stringent requirements of the following military documents:

MIL-M-38510—General Specifications for Microcircuits

MIL-Q-9858A—Quality Program Requirements

MIL-STD-883—Test Methods and Procedures for Microelectronics

Outlined below are the Teledyne Philbrick Production Processing procedures per method 5004 referencing MIL-STD-883 inspection and test documentation as applicable.

Standard micropackaged linear microcircuits available with optional MIL-TYPE processing include Models Q25AH (page 17), 1412 (page 19), 141410 (page 21). Also available with optional MIL-TYPE processing are Series 1319, 1321, 1322, 1323, 1324, 1339, 1402, 1421, 1422, 1423, 1425, 1426, 1427, and 1429.

MIL-type micropackaged data-converters are detailed on pages 38 and 39.

For detailed information on Philbrick's high reliability products send for publication number M-883, which is available by completing the post-paid card at the rear of this catalog or contact factory directly.

MANUFACTURING, SCREENING, AND INSPECTION FOR "MIL-TYPE" MICROCIRCUITS

Screen	883 - Method - 5004, Class B
Internal Visual (Pre-Cap)	2010 - Test Condition - B
Stabilization Bake	1008 - Test Condition - B (125°C)
Temperature Cycling	Method 1010, Test Condition - B (–55 to +125°C)
Constant Acceleration	Method - 2001 Test - Condition - "D" - 20,000 G's Y1 - Only ①
Seal a. Fine b. Gross	Method - 1014 a. Test Cond. - "A" P_E = 5 Atmospheres ② t_1 = 1 Hour t_2 = 30 Minutes Leak - Rate @ 5×10^{-8} cc/Sec b. Fluorocarbon Gross Leak
Burn-In Test	Method - 1015 168 Hours @ 125°C
Final Electrical Tests	Per Unit Electrical Specifications
External - Visual	Method - 2009

Notes:

1. (a.) 14-Pin Dip Units: Test Cond "B," 10,000 G's
   (b.) 24-Pin Dip Units and Model 1412: Test Cond. "A," 5,000 G's
2. 24-Pin Dip Units and Model 1412: 30 P.S.I.

MARKETING & SALES... providing the services you need

No matter where you are located in the world, you may place your order directly with us or through your nearest Philbrick Engineering Representative. (Note: If we do not yet have a representative in your country, please contact us directly). REPRESENTATIVES STOCK AMPLE QUANTITIES OF MANY STANDARD PRODUCTS, THUS CAN OFFER SAME-DAY DELIVERY. Prices listed in this catalog are F.O.B. Factory, Dedham, Massachusetts, U.S.A.; quotations on custom items, quantity orders, and other price information will be furnished by your local representative on request. Quotations are normally valid for thirty days.

To Help Us Process Your Order Quickly

Please specify model numbers and model names. For example: "Model 1427, Microcircuit Operational Amplifier" or "Model 4103, A/D Converter." Be sure to include the prefix or suffix on certain model numbers to identify special versions of the product.

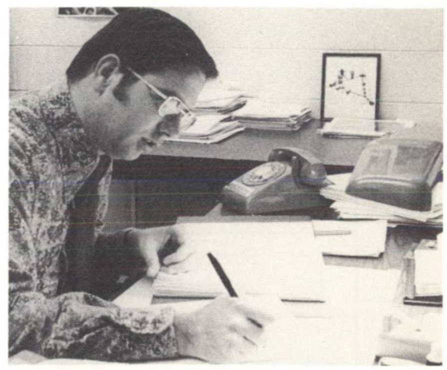
If your purchase order is a confirmation of an advance verbal order, it should be sent to the office where the advance order was placed. All confirmations should be marked "CONFIRMATION ONLY – DO NOT DUPLICATE."

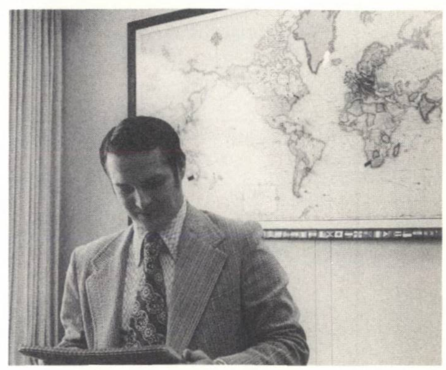
Acknowledgements will be sent out promptly by us for United States and Canadian orders on Teledyne Philbrick's standard acknowledgement forms.

MODIFICATIONS TO EQUIPMENT – Special identification markings and other minor modifications can generally be made available at a slight increase in price and delivery time. Your inquiries and specifications should be directed to your Philbrick Engineering Representative.

Regarding Shipment of Your Order

Shipments to destinations within the United States are normally made directly from the factory in Dedham, and are billed F.O.B. Dedham, Massachusetts.





Local representatives should be contacted first for small quantity purchases as the required units may be available from their stock. Shipments to other parts of the world are from the local representative's stock or directly from the factory.

Terms and Conditions of Sale

The minimum order accepted by Philbrick is $25.00. On all orders, unless alternative arrangements have been made in advance, payment is due NET 30 DAYS following date of shipment. Foreign payments and terms are arranged on an individual basis by Philbrick's International Sales Department.

Warranty

Limitation of Liability. Our goods are warranted by us to be free from defects of material or manufacture and to conform to the applicable published ratings and characteristics in effect at the time of shipment. Our liability under such warranty is limited to replacing or repairing, at our option, any goods found to be defective in such respects which are returned to us transportation prepaid within one year from the date of shipment. In no event shall we be liable for collateral or consequential damages. This warranty shall not apply to any goods which have been subjected to misuse, improper installation, repair, alteration, neglect, accident, inundation, fire or operation outside their published maximum ratings. We will have the right of final determination of the cause and existence of any defect under this warranty.

Repairs or Replacement

In accordance with the conditions of the Warranty Statement, we ask that all apparently out-of-order equipment be returned to us, whether repairable or not, so that what we learn from any units found to have defects may be applied toward product improvements and new product designs.

If for any reason you wish to return equipment to us, please contact the Teledyne Philbrick sales office for a "Return Materials Authorization Form" **before** returning the equipment. Written authorization must first be obtained before returning any merchandise. Proceed according to the instructions on the RMA form.

To expedite handling of your equipment, please enclose a copy of a letter stating model number, model name, serial number, date code, the detailed reason for return, the applications circuit diagram (if possible), any applicable purchase order number, and your exact return address. The original of that letter should be addressed to Sales Department, Teledyne Philbrick, Allied Drive at Route 128, Dedham, Massachusetts 02026.

If any Philbrick unit requiring repair or replacement is a critical component or is part of a System requiring minimum down-time, please notify your Philbrick Engineering Representative immediately. He is often able to arrange for the loan of a temporary replacement unit.

Data Sheets

Each product manufactured by Philbrick is described in depth on an individual technical bulletin which includes electrical performance, physical and mechanical specifications, as well as descriptive data and circuit diagrams for employment of the device in typical applications.

With each shipment of equipment, a complete set of technical data is enclosed.

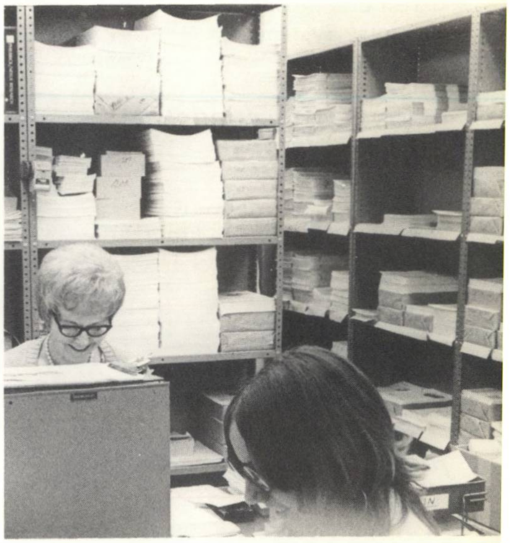
Applications Bulletins

Concise, informal sheets released periodically to illustrate salient, useful, and often new applications.

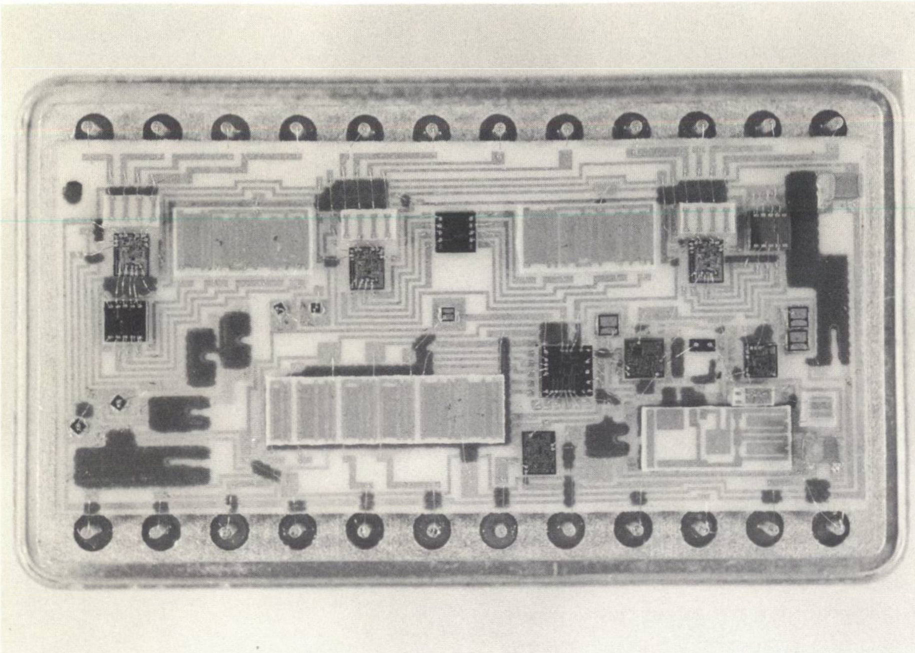
Short Form Supplementary Catalogs

Useful, comparative summaries of product families can be found in short form catalogs. They will be made available between catalog release dates, for all new instrumentation developed by Philbrick.

NOTE: the reply cards at the back of this catalog may be used to request specific literature and add your name to our mailing list if you wish.



NEW PRODUCTS FROM TELEDYNE PHILBRICK



4050
MICROCIRCUIT D/A CONVERTERS

- 8/10/12-bit Resolution
- 0.8 ppm/°C Nonlinearity T.C.
- −55 to +125°C Temp. Range
- 2 μs Settling Time to ½ LSB
- Voltage or Current Output
- Hermetically Sealed
- Complete and Self-Contained
- Feature Philbrick's Proprietary Quad Switch

□ Precision Voltage Source
□ Test Equipment
□ Display Systems

3420
MONOLITHIC CURRENT QUAD SWITCH

- 16-bit Accuracy
- 0.5 ppm/°C Nonlinearity T.C.
- 30 nSec Settling to Within 0.01%
- 3 nSec Switching Speed
- Low Leakage
- Operates over +5 to ±15 V
- I_{CBO} of 6 pA

□ D/A and A/D Converters
□ Meter Drive
□ x - y Recorders
□ Programmable Voltage Sources

4253 and 425301
LOW DRIFT FET INSTRUMENTATION AMPLIFIERS

- Ultra High Z_{in} -10^{13} Ω
- Low Drift −1 μV/°C, Max.
- High CMRR −110 db min. to 100 Hz
- Low Noise −2 μV p.p
- Low Bias Current −10 pA, Max.
- Adj. Gain, 1 — 5000

□ Low Level Instrumentation
□ High Resolution Control Loops
□ High Impedance Sensors
□ Pressure Transducers
□ Bridge Amplifiers
□ Biomedical Engineering

4853
HIGH SPEED SAMPLE-HOLD AMPLIFIER

- 1 μs Acquisition Time to 0.01% max.
- 300 nsec Settling Time to 0.01%
- 20 kHz Bandwidth
- 0.005% Linearity
- 1 mV maximum Feedthrough
- ±1 nSec max. Aperature Uncertainty Time

□ Data Acquisition Systems
□ A/D Converters
□ D/A Converters
□ Deglitch Circuits

4028 and 4029, 8 and 10 bit
MULTIPLYING D/A CONVERTERS

- Settling Time: 3 μSec
- Feedthrough: −60 dB @ 10 kHz
- Reference ±10 V @ 80 kHz
- Gain TC ±25 ppm/°C
- PSRR ±0.002%/%ΔV_S

□ CRT Character Display
□ Variable Gain Amplifier
□ Vector Generation
□ Digital to Synchro Conversion
□ Test Systems

4701, 4703, and 4705
FREQUENCY-TO-VOLTAGE CONVERTERS

	4701	4703	4705
• F.S. Output	10 kHz	100 kHz	1 MHz
• Resolution	>13-bits	>13-bits	>13-bits
• Linearity	0.008%	0.015%	0.02%
• Stability, ppm/°C	±27	±44	±47

- High Noise Rejection
- DTL/T²L output; 10-load fanout

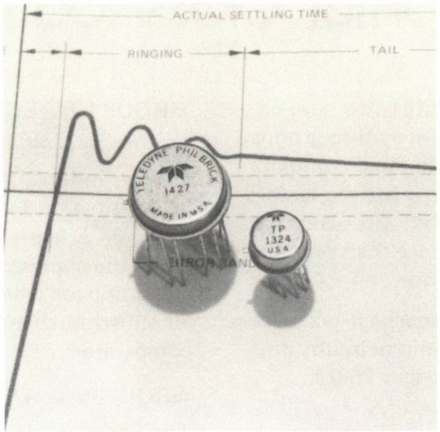
▫ Remote control or monitoring
▫ 2-wire digital transmission
▫ Electronic testing
▫ Magnetic tape recording
▫ Telemetering
▫ Isolation
▫ Servo loops
▫ Arithmetic operations
▫ Synchronous speed control

4702 and 4704
FREQUENCY-TO-VOLTAGE CONVERTERS

	4702	4704
• F.S. Input for 10 V out	10 kHz	100 kHz
• Linearity	0.008%	0.006%

- Accept DTL/T²L, HNIL, Sine Square or Triangular Wave Inputs
- Adjustable Hysterisis for use with small signals
- 20 mA Output Rating

▫ Magnetic Pickups
▫ Optical Pickups
▫ Phase Locked Loops
▫ Telemetry Systems
▫ Frequency Monitors
▫ Remote Data Transmission
▫ Tachometers
▫ Flow Meters
▫ Broadband FM Discriminators
▫ Doppler Sonar & Radar
▫ Frequency vs. Amplitude X-Y Plots



1324/1427
FAST SETTLING MICROCIRCUITS

1324
- Fast Settling - 1 μs to 0.01%
- Low E_{OS}TC - 15 μV/°C (132401)
- Pin compatible with 715 types
- Latch-up proof

▫ Fast Settling Amplifiers & Buffers
▫ 12-bit Digital-to-Analog Converters
▫ High Speed Multiplexer Amplifiers
▫ Current-to-Voltage Conversion
▫ Data Converter Deglitchers

1427
- Fast Settling - 1.5 μs to 0.01%
- Hermetically Sealed - Meets Mil Std 883
- Fully Differential FET
- Low Bias Current

▫ Data Converters
▫ Sample-and-Hold
▫ Precision Integrators
▫ Pulse Amplifiers
▫ Charge Amplifiers

1420 SERIES
FET MICROCIRCUITS

- 1421 General Purpose, Economy High CMRR/Low Bias Current
- 1422 Economy Wideband 5 MHz GBW/15 pA I_{bias}
- 1423 Low Voltage Drift 1 μV/°C E_{OS}TC/–10 pA I_{bias}
- 1424 Lowest Price FET 6 V/μs Slew Rate/50 pA I_{bias}
- 1425 Low Bias Current 5 pA I_{bias}/ 1 mV E_{OS}
- 1426 Low Voltage Drift 5 μV/°C E_{OS}TC/ 1 mV E_{OS}
- 1427 - Fast Settling
- 1428 Economy "Micro Module" Herm Seal/5 pA I_{bias}
- 1429 Ultra-Low Bias Current 0.25 pA I_{bias}/1 mV E_{OS}

4454 and 4455
PRECISION MULTIPLIERS/DIVIDERS

	4454	4455
• High Accuracy	0.5%	0.25%

- 50 kHz full Power Bandwidth
- 5 mA Output Current
- 0.01%/°C Scale Factor T.C. max.(4455)
- Short Circuit Protection

4456 and 4457
WIDEBAND MULTIPLIERS/DIVIDERS

	4456	4457
• High Accuracy	1%	0.5%

- Wide Bandwidth 5 MHz dB power; 1 MHz full power freq.
- 1% max. Phase Shift at 300 kHz
- 10 mA Output Current

4112, 4113, 4114
ECONOMY A/D CONVERTERS

- High Speed: <60 μs for 12-bits
- High Stability: ±20 ppm/°C
- Unipolar & Bipolar Input
- Serial & Parallel Output

▫ Data Acquisition Systems
▫ Test & Measuring Equipment
▫ Telemetering Systems

4024, 4025, 4026, 4027
ECONOMY D/A CONVERTERS

- 12-bit Resolution
- 200 ns Settling Time
- BCD - 4026, 4027
- Voltage or Current Output
- TTL/DTL Compatible
- Internal Reference

▫ Display Systems
▫ Test Equipment
▫ Instrumentation

LINEAR PRODUCTS

Operational Amplifier Classification

To aid in the selection of the proper amplifier, we have classified both discrete and microcircuit amplifiers into groups according to their salient specifications and most common applications. The group explanations below list the factors which determine the amplifier classification. Cross references for amplifiers considered to be in more than one category are listed with the group specifications.

For those applications where only a micropackage will suffice, we have listed the specifications for FET microcircuits on pages 24-25 and bipolar microcircuits on pages 26-27.

GROUP I – GENERAL PURPOSE – MODERATE PERFORMANCE (Pages 14-15)

Amplifiers in this group are best suited where moderate specifications of voltage drift, current drift, input impedance, and bandwidth are acceptable. The voltage drift range will be from 5 μV/°C to 30 μV/°C and current drift in the range of 0.2 nA/°C to 3 nA/°C. Typical numbers for bandwidth are 1 MHz to 2 MHz and frequency for full output of 10 kHz to 20 kHz. Applications for this group are general, such as inverters, followers as impedance buffers, adders, or amplifiers to be used with non-linear modules.

GROUP II – LOW BIAS CURRENT, HIGH INPUT IMPEDANCE (Pages 16-17)

FET input amplifiers and parametric (varactor bridge) amplifiers generally appear in this classification. The amplifiers in this group are best suited for impedance levels above 100 kΩ. The high input impedance reduces loading errors due to source resistance and the low leakage currents at the inputs provide for minimum error referred to the output. Applications include integrators, electometers, current to voltage converters, sample and hold amplifiers and low level logarithmic amplifiers. Parametric amplifiers such as the 1702 and 170201 are the ultimate in low bias current op-amps. They will resolve signal levels as low as 10^{-15} amps with source impedance levels up to 10^{14} Ω, and are best suited to measure low frequency, low level signals in such applications as electrometers and seismograph amplifiers.

GROUP III – LOW VOLTAGE DRIFT (Pages 18-19)

Amplifiers in this group have the lowest voltage drift due to changes in time, temperature, and power supply variation. The temperature coefficient will be in the range of 0.1 μV/°C to 5 μV/°C, with the lowest temperature coefficients appearing in the chopper-stabilized amplifiers. Applications for this group are where low level signals are to be resolved or amplified, such as low level signal conditioning and low level comparators.

GROUP IV – WIDEBAND, FAST RESPONSE (Pages 20-21)

Important specifications for amplifiers in this class are gain-bandwidth product, frequency for full output, slewing rate, settling time, and overload recovery. Amplifiers in this group have a unity gain bandwidth of greater than 10 MHz. Applications include high speed A-D and D-A conversion, sample-and-hold circuits, and high speed comparators.

GROUP V – SPECIAL PURPOSE (Pages 22-23)

Special purpose amplifiers include low power drain (micropower, battery operated) wide supply voltage range; high voltage, and high output current types. Individual data sheets show specific applications.

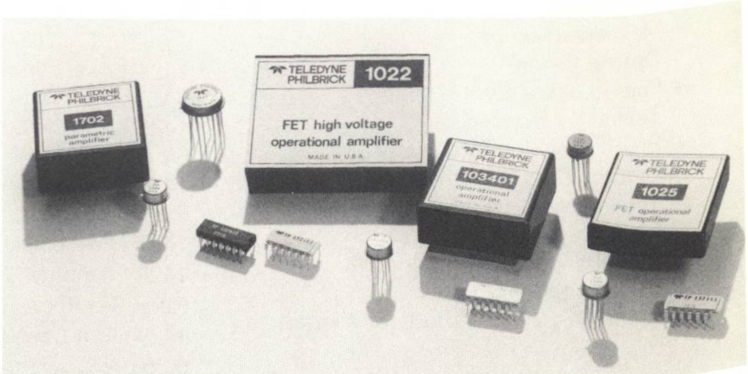
MICROCIRCUITS

FET Input

These low priced, high reliability amplifiers are designed for high impedance applications where low error currents are important. This comprehensive line will optimize most circuit designs with a minimum of effort. All units are pin compatible with the popular 741 amplifier types and require no additional stabilizing networks. The complete line of FET microcircuits is listed on pages 24 and 25 as well as individually specified under the main group headings.

BIPOLAR Input

These amplifiers have the low cost and high reliability of the 741 types plus high performance. For optimizing new designs, or updating old ones, these units are the perfect choice. Specifications are listed under the major headings, and collectively on pages 26-27.



Selecting Operational Amplifiers by Salient Parameter

Often times the selection of the right amplifier means studying many columns of data to choose the right combination of specifications to suit a particular application. To make the selection process easier we have listed in the reference chart below Philbrick's high performance amplifier's according to their optimized parameters. If more relaxed specification are acceptable, check those amplifiers detailed under the broader categories of General Purpose, Low Bias Current, Low Drift, Wideband, or special purpose detailed on the following pages.

			DISCRETE MODELS	MICROCIRCUIT MODELS
OUTPUT RANGE	Voltage, ⩾20 V		1005, 1022, 1034	
	Current, ⩾30 mA		1008, 1016, 1017, 1025	
GAIN	Rated load, ⩾200 k		1020, 1022, 1028, 1700, 1701, 1703	1323, 1412
FREQUENCY RESPONSE (Inverting)	Small signal (unity gain, open loop), ⩾10 MHz		1025, 1027, 1030, 1700	1317, 1321, 1322, 1324, 141410
	Large signal: full output ⩾500 kHz		1016, 1025, 1027, 1030, 1700	1321, 1322, 141410
	Slew rate ⩾50 V/μSec		1016, 1025, 1027, 1030, 1700	1322, 141410
	Settling time ⩽1.5 μSec to 0.01%		1025, 1027, 1030	1321, 1322, 1324, 1427, 141410
INPUT VOLTAGE RANGE	Common mode (dc linear operation), ⩾20 V		SP2A, 1005, 1016, 1022, 1034, 1702	1402
	Differential (between inputs), ⩾40 V		1005, 1016, 1022, 1702	1402
	Common mode rejection ratio (dc) ⩾100,000		SP2A, 1016, 1020, 1021, 1022, 1023, 1702	1319, 1321, 1323, 1324, 1423
INPUT VOLTAGE OFFSET	Initial (without external trim) ⩽2 mV		1020, 1022, 1023, 1700, 1701, 1703	140201, 1412, 1423, 1425, 1426, 1427, 1428, 1429
	Vs. Temperature ⩽5 μV/°C		1020, 1023, 1700, 1701, 1703	1319, 1412, 1423, 1426
	Vs. Time ⩽25 μV/day		1020, 1700, 1701, 1703	1319, 1412, 1426
	Vs. Power supply ⩽10 μV/V		1016, 1022, 1700, 1701, 1702, 1703	1319, 1323, 1324, 1412, 1423
INPUT BIAS CURRENT	Initial ⩽1 pA		SP2A, 1029, 1702	1429
	Vs. Temperature ⩽3 pA/°C slope @ 25°C		SP2A, 1021, 1023, 1029, 1700, 1702, 1703	1402, 1425, 1429
	Vs. Power Supply		SP2A, 1021, 1022, 1029, 1700, 1701, 1702, 1703	1402, 1421, 1422, 1425, 1426, 1428, 1429
	Vs. Time		SP2A, 1029, 1700, 1701, 1702, 1703	1402, 1429
	Difference (tracking)		SP2A, 1021, 1023, 1026, 1029, 1702	1425, 1429
INPUT IMPEDANCE	Differential ⩾10^{12} Ω		SP2A, 1021, 1023, 1029, 1702	1402, 1429
	Common mode ⩾10^{12} Ω		SP2A, 1021, 1023, 1029, 1702	1423, 1427, 1429, 141410
NOISE (Referred to input)	Flicker (0.016 to 1.6 Hz)	Voltage p-p ⩽1 μV	SP2A, 1020, 1021, 1023, 1028, 1034, 1700, 1701, 1703	1319, 1421, 1426, 140410
		Current p-p ⩽0.2 pA	SP2A, 1006, 1021, 1023, 1025, 1029, 1030, 1702	1402, 1429
	Midband (1.6 to 160 Hz)	Voltage rms ⩽1 μV	SP2A, 1017, 1025, 1030, 1700, 1703	1319, 1321, 1322, 140410
		Current rms ⩽0.2 pA	SP2A, 1006, 1025, 1029, 1030, 1702	1422, 1429
	Broadband (160 Hz to 16 kHz)	Voltage rms ⩽1 μV	1005, 1016, 1017	1319, 1321, 1322, 140410
		Current rms ⩽2 pA	1022, 1026, 1029	1402, 1429
POWER REQUIREMENT	Voltage range		1006, 1022, 1034	1323, 1402, 140410
	Current: quiescent ⩽1 mA		1006	1323, 1402, 140410
TEMPERATURE	Operating (−55°C to +125°C)			131901, 132102, 132201, 132302, Q25AH

Group 1. General Purpose

			DISCRETE		MICROCIRCUIT

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

				1024 Economy, 20 mA	1028 General Purpose	1421 / 142101 / 142102 FET, General Purpose
OUTPUT RANGE	E_O	Voltage, min		±10 V	±10 V	±10 V
	I_O	Current, min		±20 mA	±5 mA	±10 mA
GAIN	A_O	dc open loop, rated load, min		50,000	250,000	50 | 100 | 100 k [1]
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min		2 MHz (typ.)	1 MHz	1 MHz
	f_s	Large signal: full output (undistorted), min		130 kHz (typ.)	70 kHz (typ.)	35 kHz (typ.)
	f_p	full output (p-p), min		250 kHz (typ.)	100 kHz	50 kHz
	s_r	Slew rate, min.		6 V/µSec	6 V/µSec	3 V/µSec
	t_s	Settling time (0.1%)		5 µSec	5 µSec	3 µSec [2]
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min		±10 V	±10 V	±12 V
		(fault), abs max		±15 V	±15 V	±15 V
	CMRR	Common mode rejection ratio (dc), min.		20,000 (typ.)	10,000	4 | 4 | 10 k
INPUT VOLTAGE OFFSET	E_{os}	Initial (without ext. trim) @25 °C, max		±10 mV	--	±15 mV
	R_{os}	Zero adjustment		10 kΩ rhst.	50 kΩ rhst.	10 kΩ pot
	$E_{os}TC$	Vs. Temperature Range, max		±20 µV/°C	±20 µV/°C	50 | 50 | 25 µV/°C
	$\Delta E_{os}/\Delta t$	Vs. Time (per day)		±10 µV	±10 µV	±10 µV
	PSRR	Vs. Power Supply		±100 µV/V	±100 µV/V	±100 µV
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max		±50 nA	+35 nA	−50 | −15 | −10 pA
	I_BTC	Vs. Temperature Range, max		±0.6 nA/°C	±0.5 nA/°C	doubles ea. +10 °C
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply		±1 nA/V	±3 nA/V	±1 pA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)		±0.5 nA	±0.5 nA	±1 pA
	I_D	Difference (tracking)		±25 nA	3 nA	±25 | ±10 | ±5 pA
INPUT IMPEDANCE	Z_D	Differential		1 MΩ || 6 pF	1MΩ || 5 pF	10^{12} Ω || 3 pF
	Z_{CM}	Common mode		50 MΩ || 6 pF	1000 MΩ || 5 pF	10^{12} Ω || 3 pF
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6)	Voltage p-p	7 µV	1 µV	4 µV
	i_n		Current p-p	34 pA	20 pA	0.5 pA
	e_n	Midband (1.6 to 160 Hz)	Voltage rms	2 µV	2 µV	2 µV
	i_n		Current rms	22 pA	14 pA	0.5 pA
	e_n	Broadband (160 Hz to 16 kHz)	Voltage rms	2 µV	2 µV	3 µV
	i_n		Current rms	7 pA	4 pA	0.2 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)		±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±5 to ±20 V)
	$\pm I_{CC}$	Current: quiescent (full load), max		±9 mA (±29 mA)	±5 mA (±9 mA)	±2.8 mA (±12.8 mA)
TEMPERATURE RANGE (°C)	T_O	Operating		−25 to +85	−25 to +85	−25 to +85
	T_S	Storage		−55 to +125	−55 to +125	−65 to +150
MECHANICAL See pp., 62-69		Outline drawing		A1	A1	TO-99
		Socket		NSK-20	NSK-20	*

1. R_{LL} = 2 kΩ
2. Settling time to 0.01%, typical
3. At a gain of 100, 4.2 V/µSec at A = 1
4. Offset vs. temperature
5. Voltage rms (10 Hz to 10 kHz)
6. GBW @ A = 100

* Socket not supplied by Teledyne Philbrick.

Other amplifiers suitable for this category are:

MODEL	PAGE
1026	16
1034	22
1319	26

MICROCIRCUIT

1424 FET, Economy	1428 142801 142802 FET, Economy Micromodule			1319 131901 High Performance Low Drift		1339 133901 133902 General Purpose		
±10 V	±10 V			±10 V		±10 V		
±5 mA	±5 mA			±5 mA		±5	10	10 mA
20,000	100,000			50,000		15	40	50 k
1 MHz	1 MHz			1 MHz (typ.)		100 MHz (typ.) ⑥		
70 kHz (typ.)	35 kHz (typ.)			8 kHz		350 kHz (typ.) ③		
100 kHz (typ.)	50 kHz			10 kHz (typ.)		500 kHz (typ.) ③		
6 V/μSec	3 V/μSec			0.6 V/μSec (typ.)		34 V/μSec ③		
3 μSec ②	3 μSec ②			––		––		
±10 V	±12 V			±12 V		±11 V		
±15 V	±15 V			±15 V		±15 V		
3,200	4	4	10 k	100,000 (typ.)		10,000		
±50 mV	±2	1	1 mV	±5	2 μV	±7.5	7.5	3 mV
10 kΩ pot	––			10 kΩ pot		100 kΩ pot		
75 μV/°C	±50	25	25 μV/°C	±25	15 μV/°C	±12	5	5 μV/°C
±50 μV	±25 μV			±5 μV		±10 μV		
±150 μV/V	±100 μV/V			±10 μV/V		±30 μV/V		
50 pA	–25	10	5 pA	+250	+50 nA	+1	0.6	0.5 μA
doubles ea. +10°C	doubles ea. +10°C			±30 pA/°C typ. ④		±200 pA/°C ④		
±2 pA/V	±1 pA/V			––		±50 nA/V		
±2 pA	±1 pA			––		±25 nA		
±0.5 pA	±10	5	2 pA	±3	2 nA	±20 nA		
10^{12} ∥ 2 pF	10^{12} ∥ 3 pF			2 MΩ ∥ 3 pF		300 kΩ		
10^{12} ∥ 2 pF	10^{12} ∥ 3 pF			100 MΩ ∥ 3 pF		40 MΩ		
3 μV	3 μV			––		––		
0.3 pA	0.3 pA			––		––		
2 μV	2 μV			––		––		
0.3 pA	0.3 pA			––		––		
3 μV	3 μV			1 μV ⑤		2 μV ⑤		
0.1 pA	0.1 pA			––		––		
±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)			±15 V (±6 to ±22 V)		±15 V (±9 to +18 V)		
±6 mA (±11 mA)	±5 mA (±10 mA)			±3 mA (±8 mA)		±7 mA (±12/17/17 mA)		
0 to +70	–25 to +85			0 to +70		0 to +70		
–65 to +150	–65 to +150			–65 to +150		–65 to +150		
TO-99	T2			TO-99		TO-99		
*	6035			*		*		

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.

Group 2. Low Bias Current/High Input Impedance

DISCRETE

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

				1026 102601 FET General Purpose	1029 102901 FET Ultra Low Bias	1021 FET High CMRR Economy
OUTPUT RANGE	E_O	Voltage, min		±10 V	±10 V	±10 V
	I_O	Current, min		±5 mA	±5 mA	±20 mA
GAIN	A_O	dc open loop, rated load, min		100,000	100,000	100,000
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min		1 MHz	1 MHz	2 MHz
	f_s	Large signal: full output (undistorted), min		100 kHz	35 kHz (typ.)	70 kHz
	f_p	full output (p-p), min		150 kHz	50 kHz	100 kHz
	s_r	Slew rate, min.		10 V/µSec	3 V/µSec	6 V/µSec
	t_s	Settling time (0.1%)		10 µSec	6 µSec [1]	10 µs
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min		±10 V	±10 V	±10 V
		(fault), abs max		±15 V	±15 V	±18 V
	CMRR	Common mode rejection ratio (dc), min.		20,000	10,000	100,000
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext.trim) @25 °C, max		––	±2 mV	––
	R_{OS}	Zero adjustment		1 kΩ rhst.	50 kΩ pot	2 kΩ rhst.
	$E_{OS}TC$	Vs. Temperature Range, max		±50 / 20 / 20 µV/°C	±50 / 25 µV/°C	±50 µV/°C
	$\Delta E_{OS}/\Delta t$	Vs. Time (per day)		±50 µV	±25 µV	±50 µV
	PSRR	Vs. Power Supply		±300 µV/V	±20 µV/V	±100 µV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max		–50 / –20 / –10 pA	–0.3 / –0.1 pA	–10 pA
	I_BTC	Vs. Temperature Range, max		doubles ea. +10 °C	doubles ea. +10 °C	doubles ea. +10 °C
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply		±5 pA/V	0.05 pA/V	±0.5 pA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)		±1 pA	±0.03 pA	±1 pA
	I_D	Difference (tracking)		±10 pA	±0.1 pA	±3 pA
INPUT IMPEDANCE	Z_D	Differential		$10^{12}\Omega \parallel 5$ pF	$10^{13}\Omega \parallel 3$ pF	$10^{11}\Omega \parallel 10$ pF
	Z_{CM}	Common mode		$10^{12}\Omega \parallel 5$ pF	$10^{13}\Omega \parallel 3$ pF	$10^{12}\Omega \parallel 10$ pF
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6)	Voltage p-p	5 µV	2.5 µV	1.5 µV
	i_n		Current p-p	0.2 pA	0.04 pA	0.1 pA
	e_n	Midband (1.6 to 160 Hz)	Voltage rms	2.2 µV	3 µV	4 µV
	i_n		Current rms	1 pA	0.05 pA	0.2 pA
	e_n	Broadband (160 Hz to 16 kHz)	Voltage rms	2.2 µV	5 µV	4 µV
	i_n		Current rms	2 pA	0.03 pA	1 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)		±15 V (±10 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)
	$\pm I_{CC}$	Current: quiescent (full load), max		±10 mA (±17 mA)	±5 mA (±10 mA)	±5 mA (±25 mA)
TEMPERATURE RANGE (°C)	T_O	Operating		–25 to +85	0 to +70	–25 to +85
	T_S	Storage		–55 to +125	–55 to +125	–55 to +125
MECHANICAL See pp., 62-69		Outline drawing		A1	E11	A1
		Socket		NSK-20	NSK-20	NSK-20

1. Settling time to 0.01%, typical.
2. 10 µV rms typical (1 Hz to 100 Hz)
3. G x BW @ A = 100
* Socket not supplied by Teledyne Philbrick

Other amplifiers suitable for this category are:

MODEL	PAGE	MODEL	PAGE
1021	16	1423	25
1023	18	1424	15
1025	20	1426	25
1027	20	1427	25
1030	20	1428	24
1421	24	1700	19
1422	25	1701	19
		1703	19

DISCRETE	MICROCIRCUIT		
1702 **170201** **Differential** **Economy Parametric**	**1425** **142501** **142502** **FET** **Low Bias Current**	**1429** **142901** **142902** **FET Ultra Low Bias**	**Q25AH** **FET** **High Reliability** **(Premium)**
±10 V	±10 V	±10 V	±11 V
±5 mA	±5 mA	±5 mA	±2.2 mA
100,000	100,000	20 40 40 k	20,000
1 kHz	1 MHz	500 kHz	30 MHz
40 Hz	35 kHz (typ.)	35 kHz (typ.)	100 kHz ③
50 Hz	50 kHz	50 kHz	167 kHz
2.5 V/ms	3 V/μSec	3 V/μSec	8 V/μSec
––	3 μSec	5 μSec	––
±100 V	±12 V	±10 V	±10 V
±200 V	±10 V	±15 V	±15 V
100,000	10,000	10,000	5,000
±5 mV	±2 1 1 mV	±2 1 2 mV	±10 mV
50 kΩ pot	10 kΩ pot	10 kΩ pot	250 kΩ
±30 10 μV/°C	±50 25 10 μV/°C	±90 30 60 μV/°C	±55 μV/°C
±20 μV	±25 μV	±10 μV	±50 μV
±20 μV/V	±100 μV/V	±100 μV/V	±70 μV/V
±0.005 pA	–10 –5 –5 pA	–1 –0.5 –0.25 pA	–150 pA
±0.0002 pA/°C	doubles ea +10 °C	doubles ea. +10 °C	doubles ea. +10 °C
±0.0005 pA/V	±1 pA/V	±1 pA/V	±10 pA/V
±0.001 pA	±1 pA	±1 pA	±3 pA
±0.003 pA	±5 2 2 pA	±0.3 0.1 0.1 pA	±10 pA
3 x 10^{11} Ω ‖ 15 pF	10^{12} Ω ‖ 3 pF	10^{13} Ω ‖ 3 pF	10^{11} Ω
10^{14} Ω	10^{12} Ω ‖ 3 pF	10^{13} Ω ‖ 3 pF	10^{11} Ω
10 μV ③	3 μV	2.8 μV	5 μV
––	0.3 pA	0.04 pA	0.2 pA
10 μV	2 μV	2.9 μV	2 μV
––	0.3 pA	0.05 pA	1 pA
200 μV	3 μV	4.8 μV	2 μV
––	0.1 pA	0.03 pA	3 pA
±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18V)
+13, –8mA (+18, –13mA)	±2.8 mA (±7.8 mA)	±5 mA (±10 mA)	±7.6 mA (±9.8 mA)
0 to +70	–25 to +85	0 to +70	–55 to +125
–55 to +125	–55 to +150	–65 to +150	–62 to +150
E5	TO-99	TO-99	TO-8
NSK-20	*	*	US-Q

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.

Group 3. Low Voltage Drift

DISCRETE

Specifications listed left to right correspond to model numbers top to bottom above.

				1020 102001 102002 102003 Economy Low Drift Differential	1023 102301 FET, Low Drift	1700 170001 170002 Wideband Chopper
OUTPUT RANGE	E_O	Voltage, min		±10 V	±10 V	±10 V
	I_O	Current, min		±5 mA	±20 mA	±20 mA
GAIN	A_O	dc open loop, rated load, min		200 k	100,000	10^8
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min		0.5 MHz	2 MHz	16 MHz
	f_s	Large signal: full output (undistorted), min		5 kHz	100 kHz	1 MHz
	f_p	full output (p-p), min		10 kHz	150 kHz (typ.)	1.2 MHz
	s_r	Slew rate, min.		0.3 V/µSec	6 V/µSec	100 V/µSec
	t_s	Settling time (0.1%)		40 µSec ①	10 µSec	4 µSec (max.)
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min		±10 V	±10 V	--
		(fault), abs max		±15 V	±18 V	--
	CMRR	Common mode rejection ratio (dc)		100,000 (min.)	100,000 (min.)	--
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext trim) @25 °C, max		±3 | 0.5 | 0.5 | 0.6 mV ②	±700 µV ②	±50 µV
	R_{OS}	Zero adjustment		supplied	supplied	1 MΩ pot
	$E_{OS}TC$	Vs. Temperature Range, max		±5 | 1.5 | 0.5 | 0.25 µV/°C ②	±5 | 2 µV/°C ②	±1 | 0.5 | 0.2 µV/°C
	$\Delta E_{OS}/\Delta t$	Vs. Time (per day)		±5 µV	±20 µV	±1 µV
	PSRR	Vs. Power Supply		±50 µV/V	±100 µV/V	±10 µV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max		±25 nA	-20 pA	±100 pA
	$I_B TC$	Vs. Temperature Range, max		±500 pA/°C	doubles ea. +10 °C	±2 pA/°C ③
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply		±0.7 nA/V	±1 pA/V	±20 pA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)		±2 nA	±1 pA	±2 pA
	I_D	Difference (tracking)		±5 nA (max.)	±3 pA	--
INPUT IMPEDANCE	Z_D	Differential		4 MΩ ‖ 8 pF	10^{11} Ω ‖ 10 pF	500 kΩ ‖ 66 pF
	Z_{CM}	Common mode		1000 MΩ ‖ 8 pF	10^{12} Ω ‖ 10 pF	--
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6)	Voltage p-p	2 µV	1.5 µV	3 µV
	i_n		Current p-p	50 pA	0.1 pA	6 pA
	e_n	Midband (1.6 to 160 Hz)	Voltage rms	3 µV	4 µV	1 µV
	i_n		Current rms	6 pA	0.2 pA	20 pA
	e_n	Broadband (160 Hz to 16 kHz)	Voltage rms	3 µV	4 µV	2.3 µV
	i_n		Current rms	6 pA	1 pA	350 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)		±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)
	$\pm I_{CC}$	Current: quiescent (full load), max		±12 mA (±17, −12 mA)	±6 mA (±26 mA)	±12 mA (±31 mA)
TEMPERATURE RANGE (°C)	T_O	Operating		-25 to +85	-10 to +60	-25 to +85
	T_S	Storage		-55 to +125	-55 to +125	-55 to +100
MECHANICAL See pp., 62-69		Outline drawing		A1	A1	E4
		Socket		NSK-20	NSK-20	6023

1. Settling time to 0.01%, typical.
2. With external trim resistor supplied
3. ±1 pA/°C, max. (0 to +60 °C)
4. Offset vs. temperature
5. Voltage rms (10 Hz to 10 kHz)
* Socket not supplied by Teledyne Philbrick

DISCRETE		MICROCIRCUIT			
1701 **170101** **General Purpose Chopper**	**1703** **170301** **Economy Chopper**	**1426** **142601** **142602** **142603** **FET, Low Drift**	**1423** **142301** **142302** **FET, Low Drift**	**1319** **131901** **Premium Low Drift**	**1412** **Mini Chopper Stabilized Microcircuit**
±12 V	±10 V	±10 V	±10 V	±10 V	±12 V
±5 mA	±5 mA	±5 mA	±5 mA	±5 mA	±5 mA
10^7	10^6	100,000	100,000	50,000	10^6
1 MHz (typ.)	1 MHz (typ.)	1 MHz	3 MHz (typ.)	1 MHz (typ.)	1 MHz (typ.)
20 kHz	4.5 kHz	35 kHz (typ.)	70 kHz (typ.)	8 kHz	14 kHz
30 kHz	7 kHz (typ.)	50 kHz	100 kHz	10 kHz (typ.)	20 kHz
1.2 V/µSec	0.25 V/µSec	3 V/µSec	6 V/µSec	0.6 V/µSec (typ.)	1.2 V/µSec (min.)
——	——	3 µSec	10 µSec	——	——
——	——	±12 V	±10 V	±12 V	——
——	——	±15 V	±15 V	±15 V	——
——	——	4 10 10 10 k	100,000	100,000 (typ.)	——
±15 µV	±40 15 µV	±2 1 1 1 mV	±2 1 1 µV	±5 2 µV	±25 µV
50 kΩ pot	50 kΩ pot	10 kΩ pot	1 kΩ pot	10 kΩ pot	50 kΩ pot
±0.25 0.1 µV/°C	±1 0.3 µV/°C	±50 25 10 5 µV/°C	±5 2 1 µV/°C	±25 15 µV/°C	±0.5 µV/°C
±5 µV/yr	±5 µV/yr	±10 µV	±10 µV	±5 µV	±1 µV/mo
±0.2 pV/V	±1 µV/V	±100 µV/V	±10 µV/V	±10 µV/V	±0.25 µV/V
±50 pA	±50 pA	−25 10 25 25 pA	−10 pA	+250 +50 nA	±100 pA
±1 pA/°C	±2 0.5 pA/°C	doubles ea. +10°C	doubles ea. +10°C	±30 pA/°C typ. ④	±5 pA/°C
±2 pA/V	±5 pA/V	±1 pA/V	±5 pA/V	——	±3 pA/V
±10 pA/yr	±10 pA/yr	±1 pA	±1 pA	——	±1 pA/mo
——	——	±10 5 10 10 pA	±2 pA	±3 2 nA	——
500 kΩ ‖ 100 pF	800 kΩ ‖ 100 pF	10^{11} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	2 MΩ ‖ 3 pF	500 kΩ ‖ 100 pF
——	——	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	100 MΩ ‖ 3 pF	——
1 µV	1 µV	4 µV	5 µV	——	5 µV
5 pA	3 pA	0.5 pA	0.2 pA	——	4 pA
2 µV	2 µV	2 µV	2 µV	——	5 µV
5 pA	6 pA	0.5 pA	0.3 pA	——	5 pA
5 µV	2 µV	3 µV	3 µV	1 µV ⑤	7 µV
25 pA	——	0.2 pA	2 pA	——	30 pA
±15 V (±8 to ±20 V)	±15 V (±12 to ±18)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±6 to ±22 V)	±15 V (±8 to ±20 V)
±3 mA (±8 mA)	±5 mA (±10 mA)	±2.8 mA (±7.8 mA)	±10 mA (±15 mA)	±3 mA (±8 mA)	+3, −5 mA (±8 mA)
−25 to +85	0 to +70	−25 to +85	0 to +70	0 to +70	−25 to +85
−55 to +125	−55 to +125	−65 to +150	−55 to +125	−65 to +150	−55 to +125
E5	E11	TO-99	S4	TO-99	A5
NSK-20	NSK-20	*	*	*	6053

Selected versions are available on all models, consult factory.

Specifications typical at 25°C with nominal power supply, unless otherwise indicated.

Group 4. Wideband/Fast Response

DISCRETE

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

			1027 / 102701 Fast FET, Differential	1025 Fast Settling FET	1030 High Slew Rate FET, Differential
OUTPUT RANGE	E_O	Voltage, min	±10 V	±10 V	±10 V
	I_O	Current, min	±20 mA	±50 mA	±20 mA
GAIN	A_O	dc open loop, rated load, min	100,000	100,000	100,000
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min	10 MHz	50 MHz	100 MHz (7) (8) (15)
	f_s	Large signal: full output (undistorted), min	500 kHz	5 MHz	5 MHz (15)
	f_p	full output (p-p), min	1 MHz	10 MHz (typ.)	10 MHz (typ.) (15)
	s_r	Slew rate, min.	60 V/μSec	500 V/μSec	850 V/μSec (typ.) (15)
	t_s	Settling time (0.01%), max.	1 μSec	300 nSec (1)	500 nSec (15)
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min	±10 V	±4 V	±10 V
		(fault), abs max	±15 V	±18 V	±18 V
	CMRR	Common mode rejection ratio (dc), min.	10,000	10,000 (typ.)	50,000
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext. trim) @25 °C, max	±15 mV (14)	±10 mV (max.)	±2 mV (max.)
	R_{OS}	Zero adjustment	1 kΩ rhst	100 kΩ	100 kΩ pot
	$E_{OS}TC$	Vs. Temperature Range, max	±50 / 15 μV/°C	±50 μV/°C	±25 μV/°C
	$\Delta E_{OS}/\Delta t$	Vs. Time (per day)	±50 μV	±50 μV	±100 μV
	PSRR	Vs. Power Supply	±300 μV/V	±100 μV/V	±200 μV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max	−50 pA	−20 pA	−20 pA
	I_BTC	Vs. Temperature Range, max	doubles ea. +10 °C	doubles ea. +10 °C	doubles ea. +10 °C
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply	±1 pA/V	±1 pA/V	±1 pA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)	±5 pA	±2 pA	±2 pA
	I_D	Difference (tracking)	±10 pA (max.)	±10 pA	±10 pA
INPUT IMPEDANCE	Z_D	Differential	10^{11} Ω ‖ 5 pF	10^{11} Ω ‖ 8 pF	10^{11} Ω ‖ 5 pF
	Z_{CM}	Common mode	10^{11} Ω ‖ 5 pF	10^{12} Ω ‖ 5 pF	10^{12} Ω ‖ 25 pF (2)
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6) — Voltage p-p	5 μV	15 μV	15 μV
	i_n	Flicker (0.016 to 1.6) — Current p-p	0.5 pA	0.1 pA	0.1 pA
	e_n	Midband (1.6 to 160 Hz) — Voltage rms	2 μV	0.5 μV	0.5 μV
	i_n	Midband (1.6 to 160 Hz) — Current rms	0.2 pA	0.1 pA	0.1 pA
	e_n	Broadband (160 Hz to 16 kHz) — Voltage rms	4 μV	3 μV	3 μV
	i_n	Broadband (160 Hz to 16 kHz) — Current rms	1 pA	1 pA	1 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)	±15 V (±12 to ±18 V)	±15 V (±12 V to ±18 V)	±15 V (±12 V to ±18 V)
	$\pm I_{CC}$	Current: quiescent (full load), max	±12 mA (±30 mA)	±40 mA (±85 mA)	±20 mA (±40 mA)
TEMPERATURE RANGE (°C)	T_O	Operating	−25 to +85	−25 to +85	−25 to +85
	T_S	Storage	−55 to +125	−55 to +125	−55 to +125
MECHANICAL See pp., 62-69		Outline drawing	A4	E5	E5
		Socket	NSK-20	NSK-20	NSK-20

1. 75 nsec to 0.1% max.
2. 5 pF negative input to common
3. Compensated for unity gain
4. For 5 Hz to 50 kHz bandwidth, e_n = 6 μV rms, typical
5. This socket not supplied by Teledyne Philbrick, available from Barnes Corp., Lansdowne, Pa.
6. Gain x Bandwidth @ A_{cl} = 5
7. Gain x Bandwidth @ A_{cl} = 10
8. Offset vs. temperature
9. Voltage rms (10 Hz to kHz)
10. 500 nsec to 0.1%
11. 300 nsec to 0.1%
12. Also available in 14 pin DIP, as the Model 132410. Consult factory.
13. R_{LL} = 2 kΩ
14. With 499 Ω, 1% MF
15. Inverting or non-inverting

* Socket not supplied by Teledyne Philbrick

MICROCIRCUIT

1324 132401 Fast Settling	1422 142201 FET, Wideband	1427 142701 FET Fast Settling	141410 FET Fast Settling	1321 132101 Wideband High Z_{in}	1322 132201 High Slew Rate
±10 V	±10 V	±10 V	±10 V	±10 V	±10 V
±10 mA	±10 mA	±10 mA	±20 mA	±10 mA	±10 mA
100,000	50,000/100,000 ⑬	100,000	100,000	80,000	5,000
8 MHz ⑮	5 MHz ⑥	6 MHz	10 MHz (typ.)	100 MHz (typ.) ⑦	20 MHz ⑦
350 kHz ⑮	100 kHz	350 kHz (typ.)	500 kHz	320 kHz	1.2 MHz
500 kHz (typ.) ⑮	130 kHz (typ.)	500 kHz (typ.)	1 MHz (typ.)	600 kHz (typ.)	2 MHz (typ.)
25 V/μSec ⑮	8 V/μSec	25 V/μSec	50 V/μSec	35 V/μSec (typ.)	80 V/μSec
1.0 μSec ③ ⑮	––	1.5 μSec	1 μSec	3.5 μSec ⑩	3 μSec ⑪
±10 V	±12 V	±10 V	±10 V	±12 V	±10 V
±15 V	±15 V	±15 V	±18 V	±15 V	±15 V
150,000	4,000	100,000	5,000 (typ.)	100,000 (typ.)	30,000 (typ.)
±10 3 mV	±15 mV	±2 1 mV	±5 mV	±5 mV	±10 mV
50 kΩ pot	10 kΩ pot	––	1 kΩ pot	100 kΩ pot	±20 kΩ pot
±30 15 μV/°C	±50 μV/°C	±50 25 μV/°C	±50 μV/°C	±30 μV/°C (typ.)	±30 μV/°C (typ.)
±50 μV	±50 μV	±25 μV	±50 μV	±15 μV	±15 μV
±10 μV/V	±100 μV/V	±200 μV/V	±500 μV/V	±30 μV/V	±30 μV/V
+300 +200 nA	-50 -15 pA	-50 -25 pA	-100 pA	+25 nA	+250 nA
±1 nA/°C	doubles ea. +10 °C	doubles ea. +10 °C	doubles ea. +10 °C	±0.8 nA/°C ⑧	±0.5 nA/°C ⑧
+0.5 nA/V	±1 pA/V	±1 pA/V	±5 pA/V	±0.2 nA/V	0.7 μA
±5 nA	±1 pA	±2 pA	±2 pA	±2 nA	±10 nA
±50 30 nA	25/10 pA	±10 pA	±10 pA	±5 nA	±20 nA
3 MΩ ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{11} Ω ‖ 3 pF	10^{11} Ω ‖ 3 pF	300 MΩ ‖ 3 pF	100 MΩ ‖ 3 pF
1000 MΩ ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{11} Ω ‖ 3 pF	1000 MΩ ‖ 3 pF	1000 MΩ ‖ 3 pF
4 μV	4 μV	8 μV	15 μV	––	––
30 pA	0.5 pA	0.3 pA	0.1 pA	––	––
1.2 μV	2 μV	3 μV	4 μV	––	––
20 pA	0.05 pA	1 pA	2 pA	––	––
3.5 μV ④	3 μV	4 μV	4 μV	1 μV ⑨	1 μV ⑨
100 pA	0.2 pA	3 pA	3 pA	––	––
±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±10 to ±18 V)	±15 V (±8 to ±22 V)	±15 V (±8 to ±20 V)
±15 mA (±25 mA)	±2.8 mA (±12.8 mA)	±15 mA (±25 mA)	±10 mA (±30 mA)	±4 mA (±14 mA)	±6 mA (±16 mA)
0 to +70	-25 to +85	-25 to +85	-25 to +85	0 to +70 -55 to +125	0 to +75 -55 to +125
-65 to +125	-65 to +150	-55 to +125	-55 to +125	-65 to +150	-65 to +150
TO-100 ⑫	TO-99	TO-8	S4	TO-99	TO-99
⑤	⑤	US-Q	⑤	⑤	⑤

Another amplifier suitable for this category is:

MODEL	PAGE
1700	18

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.

Group 5. Special Purpose

DISCRETE

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

				1005 20 V General Purpose	1022 High Voltage FET	1034 103401 20 V - 22 mA General Purpose
OUTPUT RANGE	E_O	Voltage, min		±20 V	$\pm\lvert V_{CC}-10\rvert$ V	±20 V
	I_O	Current, min		±5 mA	±20 mA	±22 mA
GAIN	A_O	dc open loop, rated load, min		50,000	1,000,000	100,000
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min		1.0 MHz	1 MHz	1 MHz
	f_s	Large signal: full output (undistorted), min		10 kHz	35 kHz (typ.)	35 kHz (typ.) ②
	f_p	full output (p-p), min		20 kHz (typ.)	50 kHz ①	50 kHz
	s_r	Slew rate, min.		1.2 V/µSec (typ.)	30 V/µSec ①	6 V/µSec ②
	t_s	Settling time (0.1%)		20 µSec	7 µSec	5 µSec
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min		±20 V	$\pm\lvert V_{CC}-15\rvert$ V	±20 V
		(fault), abs max		±26 V	±150 V	±26 V
	CMRR	Common mode rejection ratio (dc)		20,000	200,000	20,000 (min.)
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext. trim) @25 °C, max.		––	±1 mV	––
	R_{OS}	Zero adjustment		50 kΩ rhst	1 kΩ pot	50 kΩ rhst
	$E_{OS}TC$	Vs. Temperature Range, max		±20 µV/°C	±50 µV/°C	±15 / 5 µV/°C
	$\Delta E_{OS}/\Delta t$	Vs. Time (per day)		±25 µV	±100 µV	±25 µV
	PSRR	Vs. Power Supply		±100 µV/V	±10 µV/V	±50 µV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max		±25 nA	-30 pA	+50 nA
	I_BTC	Vs. Temperature Range, max		±1 nA/°C	doubles ea. +10 °C	±0.4 nA/°C
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply		±5 nA/V	±0.5 pA/V	±3 nA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)		±3 nA	±2 pA	±2 nA
	I_D	Difference (tracking)		±2 nA	±10 pA	3 nA
INPUT IMPEDANCE	Z_D	Differential		250 kΩ ‖ 6 pF	10^{11} Ω ‖ 10 pF	1 MΩ ‖ 3 pF
	Z_{CM}	Common mode		50 MΩ ‖ 5 pF	10^{12} Ω ‖ 10 pF	1000 MΩ ‖ 4 pF
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6)	Voltage p-p	5 µV	25 µV	1 µV
	i_n		Current p-p	150 pA	0.5 pA	20 pA
	e_n	Midband (1.6 to 160 Hz)	Voltage rms	1 µV	8 µV	2 µV
	i_n		Current rms	50 pA	0.2 pA	4 pA
	e_n	Broadband (160 Hz to 16 kHz)	Voltage rms	0.9 µV	5 µV	2 µV
	i_n		Current rms	40 pA	0.5 pA	10 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)		±26 V (±22 to ±28 V)	±120 V (±40 to ±150 V)	±26 V (±15 to ±35 V)
	$\pm I_{CC}$	Current: quiescent (full load), max		±7 mA (±12 mA)	±10 mA (±30 mA)	±4 mA (±26 mA)
TEMPERATURE RANGE (°C)	T_O	Operating		-25 to +85	-25 to +85	-25 to +85
	T_S	Storage		-55 to +125	-55 to +125	-55 to +125
MECHANICAL See pp., 62-69		Outline drawing		A1	G4	E11
		Socket		NSK-20	6043	NSK-20

1. E_O = ±100 V
2. Inverting mode only. f_s = 10 kHz and slew rate = 1.2 V/µSec for noninverting mode.
3. Short circuit = ±80 mA
4. Offset vs. temperature
5. Voltage rms (10 Hz to 10 kHz)
6. When inputs are less than 5 mV apart. When inputs are more than 50 mV apart quiescent current is ±3 mA.

* Socket available from Barnes Corp., Lansdowne, Pa. Not available from Teledyne Philbrick.

DISCRETE				MICROCIRCUIT		
1008 FET, 30 mA	**1017** Economy, 125 mA	**1016** High Speed, 100 mA	**1006** FET, Micropower	**140410** **140411** Micropower	**1402** **140202** FET, Battery	**1323** **132301** **132302** Low Power
±10 V	±10 V	$\pm\lvert V_{CC}-5\rvert V$	$\pm\lvert V_{CC}-1.2\rvert V$	$\pm\lvert V_{CC}-2\rvert V$	$\pm\lvert V_{CC}-2\rvert V$	±12 V
±30 mA	±125 mA	±100 mA	±1 mA	±1 mA	±2 mA	±10 mA
50,000	20,000	300,000	10,000	25,000	10,000	200,000
3 MHz	1 MHz	10 MHz (typ.)	600 kHz (typ.)	0.1 MHz	1.0 MHz	1 MHz (typ.)
140 kHz (typ.)	15 kHz	1 MHz	35 kHz (typ.)	5 kHz	50 kHz (typ.)	25 kHz
200 kHz	18 kHz	1 MHz	50 kHz	8 kHz	70 kHz	200 kHz (typ.)
10 V/µSec	1 V/µSec	60 V/µSec	0.5 V/µSec	0.12 V/µSec	3 V/µSec (min.)	10 V/µSec
6 µSec	15 µSec	1 µSec (0.01% typ.)	6 µSec	50 µSec	4 µSec	10 µSec
±10 V	±10 V	$\pm\lvert V_{CC}-5\rvert V$	$\pm\lvert V_{CC}-2.2\rvert V$	$\pm\lvert V_{CC}-2\rvert V$	$\pm\lvert V_{CC}-3\rvert V$	±11 V
±15 V	±15 V	$\pm V_{CC}$	$\pm V_{CC}$	$\pm V_{CC}$	$\pm V_{CC}$	±15 V
5,000	1,000 (min.)	100,000	2,000	50,000	6,500	200,000
——	±6 mV	——	±1 mV	±5 1 mV	±3 1 mV	±5 3 3 mV
1 kΩ rhst	1 MΩ pot	50 kΩ pot	1 kΩ pot	1 MΩ pot	1 kΩ pot	1 MΩ pot
±35 µV/°C	±45 µV/°C	±20 µV/°C	±50 µV/°C	±20 10 µV/°C	±50 10 µV/°C	±30 µV/°C
±50 µV	±10 µV	±50 µV	±25 µV	±25 µV	±25 µV	±10 µV
±50 µV/V	±50 µV/V	±10 µV/V	±200 µV/V	±10 µV/V	±400 µV/V	±10 µV/V
−100 pA	±100 nA	±10 nA	−50 pA	+30 nA	−30 pA	+40 20 20 nA
doubles ea. +10°C	±3 nA/°C	±1 nA/°C	doubles ea. +10°C	±0.5 nA/°C	doubles ea. +10°C	±0.5 nA/°C ④
±5 pA/V	±25 nA/V	±0.1 nA/V	±1 pA/V	±350 pA/V	±3 pA/V	±0.5 nA/V
±5 pA	±2 nA	±1 nA	±2 pA	±1 nA	±1 pA	±0.5 nA
±20 pA	±50 nA	±2 nA	±10 pA	±7 nA (max.)	±10 pA	±2.5 nA
$10^{11}\ \Omega \parallel 5$ pF	210 kΩ $\parallel$ 10 pF	0.5 MΩ $\parallel$ 6 pF	$10^{11}\ \Omega \parallel 6$ pF	4 MΩ $\parallel$ 10 pF	$10^{12}\ \Omega \parallel 4$ pF	2 MΩ $\parallel$ 3 pF
$10^{12}\ \Omega \parallel 6$ pF	200 MΩ $\parallel$ 4 pF	1000 MΩ $\parallel$ 6 pF	$10^{12}\ \Omega \parallel 6$ pF	100 MΩ $\parallel$ 10 pF	$10^{12}\ \Omega \parallel 10$ pF	200 MΩ $\parallel$ 3 pF
8 µV	3 µV	5 µV	6 µV	1 µV	6 µV	——
1 pA	220 pA	100 pA	0.2 pA	15 pA	0.1 pA	——
5 µV	1 µV	2 µV	2 µV	0.3 µV	2 µV	——
1 pA	60 pA	60 pA	1 pA	3 pA	1 pA	——
5 µV	1 µV	0.9 µV	3 µV	1 µV	2 µV	10 µV ⑤
3 pA	90 pA	100 pA	2 pA	3 pA	2 pA	——
±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±8 to ±28 V)	±2.7 V (±2 to ±16 V)	±4.5 V (±2 to ±18 V)	±15 V (±4 to ±24 V)	±15 V (±5.5 to ±20 V)
±10 mA (±40 mA)	±15 mA (±140 mA) ③	±25 mA (±125 mA)	±200 µA (±1.2 mA)	±75 µA (±1.2 mA)	±1.0 mA (±3.0 mA)	±80 µA (±10 mA) ⑥
−25 to +85	−25 to +85	−25 to +85	−25 to +85	−25 to +85	−25 to +85	*
−55 to +100	−55 to +125	−55 to +125	−55 to +85	−55 to +125	−55 to +125	−65 to +150
A1	A1	G1	A1	S4	TO-8	TO-99
NSK-20	NSK-20	NSK-9	NSK-20	*	US-Q	*

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.

FET Microcircuits

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

			GENERAL PURPOSE			LOW BIAS CURRENT
			1421 142101 142102 General Purpose, Low Drift	1424 Economy	1428 142801 142802 Economy Micromodule	1425 142501 142502 Low Bias Current
OUTPUT RANGE	E_O	Voltage, min	±10 V	±10 V	±10 V	±10 V
	I_O	Current, min	±10 mA	±5 mA	±5 mA	±5 mA
GAIN	A_O	dc open loop, rated load, min	50 / 100 / 100 k ①	20,000	100,000	100,000
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min	1 MHz	1 MHz (typ.)	1 MHz	1 MHz
	f_s	Large signal: full output (undistorted), min	35 kHz (typ.)	70 kHz (typ.)	35 kHz (typ.)	35 kHz (typ.)
	f_p	full output (p-p), min	50 kHz	100 kHz (typ.)	50 kHz	50 kHz
	s_r	Slew rate, min.	3 V/μSec	6 V/μSec (typ.)	3 V/μSec	3 V/μSec
	t_s	Settling time (0.01%)	3 μSec	3 μSec	3 μSec	3 μSec
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min	±12 V	±10 V	±12 V	±12 V
		(fault), abs max	±15 V	±15 V	±15 V	±10 V
	CMRR	Common mode rejection ratio (dc), min.	4 / 4 / 10 k	3,200	4 / 10 / 10 k	10,000
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext. trim) @25 °C, max	±3 mV (typ.)	±50 mV	±2 / 1 / 1 mV	±2 / 1 / 1 mV
	R_{OS}	Zero adjustment	10 kΩ pot	10 kΩ pot	——	10 kΩ pot (opt.)
	$E_{OS}TC$	Vs. Temperature Range, max	50 / 50 / 25 μV/°C	75 μV/°C	±50 / 25 / 25 μV/°C	±50 / 25 / 10 μV/°C
	$\Delta E_{OS}/\Delta t$	Vs. Time (per day)	±10 μV	±50 μV	±25 μV	±25 μV
	PSRR	Vs. Power Supply	±100 μV/V	±150 μV/V	±100 μV/V	±100 μV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max	−50 / −15 / −10 pA	−50 pA	−25 / −10 / −5 pA	−10 / −5 / −5 pA
	I_BTC	Vs. Temperature Range, max	doubles ea. +10 °C	doubles ea. +10 °C	doubles ea. +10 °C	doubles ea. +10 °C
	$\Delta I_B/\Delta V_{CC}$	Vs. Power Supply	±1 pA/V	±2 pA/V	±1 pA/V	±1 pA/V
	$\Delta I_B/\Delta t$	Vs. Time (per day)	±1 pA	±2 pA	±1 pA	±1 pA
	I_D	Difference (tracking)	±25 / 10 / 5 pA	±0.5 pA	±10 / 5 / 2 pA	±5 / 2 / 2 pA
INPUT IMPEDANCE	Z_D	Differential	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 2 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF
	Z_{CM}	Common mode	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 2 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF
NOISE (Referred to input)	e_n	Flicker (0.016 to 1.6) — Voltage p-p	4 μV	6 μV	3 μV	3 μV
	i_n	Flicker (0.016 to 1.6) — Current p-p	0.5 pA	0.3 pA	0.3 pA	0.3 pA
	e_n	Midband (1.6 to 160 Hz) — Voltage rms	2 μV	3 μV	2 μV	2 μV
	i_n	Midband (1.6 to 160 Hz) — Current rms	0.5 pA	0.3 pA	0.3 pA	0.3 pA
	e_n	Broadband (160 Hz to 16 kHz) — Voltage rms	3 μV	4 μV	3 μV	3 μV
	i_n	Broadband (160 Hz to 16 kHz) — Current rms	0.2 pA	0.1 pA	0.1 pA	0.1 pA
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V(±12 to ±18 V)
	$\pm I_{CC}$	Current: quiescent (full load), max	±2.8 mA (±12.8 mA)	±6 mA (±11 mA)	±5 mA (±10 mA)	±2.8 mA (±7.8 mA)
TEMPERATURE RANGE (°C)	T_O	Operating	−25 to +85	0 to +70	−25 to +85	−25 to +85
	T_S	Storage	−65 to +150	−55 to +150	−65 to +150	−55 to +150
MECHANICAL See pp., 62-69		Outline drawing	TO-99	TO-99	T2	TO-99
		Socket	*	*	6035	*

1. R_{LL} = 2 kΩ
2. Settling time to 0.01% max.
3. Gain x Bandwidth @ A_{cl} = 5
4. e_n = 4.2 μV rms typical from 5 Hz to 50 kHz
5. A_{cl} = 5

* Socket not supplied by Teledyne Philbrick.

—— LOW BIAS CURRENT ——►◄—— LOW VOLTAGE DRIFT ——►◄—— WIDEBAND ——►◄—— SPECIAL PURPOSE ——►

1429 / 142901 / 142902 **Ultra-low Bias Current**	1426 / 142601 / 142602 / 142603 **Low Drift**	1423 / 142301 / 142302 **Ultra-low Drift**	1422 / 142201 **FET, Wideband**	1427 / 142701 **FET, Fast Settling**	141410 **Hermetically Sealed Fast Differential FET**	1402 / 140202 **FET, Battery**
±10 V	±10 V	±10 V	±10 V	±10 V	±10 V	$\pm\|V_{CC}-2\|$V
±5 mA	±5 mA	±5 mA	±10 mA	±10 mA	±20 mA	±2 mA
20 / 40 / 40 k	100,000	100,000	50 / 100 k ①	100,000	100,000	10,000
500 kHz	1 MHz	3 MHz (typ.)	5 MHz ③	6 MHz	10 MHz (typ.)	1.0 MHz
35 kHz (typ.)	35 kHz (typ.)	70 kHz (typ.) ③	100 kHz (typ.)	350 kHz (typ.)	500 kHz	50 kHz (typ.)
50 kHz	50 kHz	100 kHz	130 kHz (typ.) ③	500 kHz (typ.)	1 MHz (typ.)	70 kHz
3 V/µSec	3 V/µSec	6 V/µSec	8 V/µSec ③	20 V/µSec	50 V/µSec	3 V/µSec
5 µSec	3 µSec	15 µSec	——	1.0 µSec	1 µSec ③	8 µSec
±10 V	±12 V	±10 V	±12 V	±10 V	±10 V	$\pm\|V_{CC}-3\|$V
±15 V	±15 V	±15 V	±15 V	±15 V	±18 V	$\pm V_{CC}$
3200 / 10 k / 10 k	4 / 10 / 10 / 10 k	100,000	4,000	10,000	5,000 (typ.)	6,500
±5 / 1 / 2 mV	±2 / 1 / 1 / 1 mV	±2 / 1 / 1 mV	±15 mV	±1 / 0.5 mV	±5 mV	±3 / 1 mV
10 kΩ pot	10 kΩ pot	1 kΩ pot	10 kΩ pot (opt.)	——	1 kΩ pot	1 kΩ pot
±90 / 30 / 60 µV/°C	±50 / 25 / 10 / 5 µV/°C	±5 / 2 / 1 µV/°C	±50 µV/°C	±50 / 25 µV/°C	±50 µV/°C	±50 / 10 µV/°C
±10 µV	±10 µV	±10 µV	±10 µV	±25 µV	±100 µV	±25 µV
±100 µV/V	±100 µV/V	±10 µV/V	±100 µV/V	±200 µV/V	±500 µV/V	±400 µV/V
−1 / −0.5 / −0.25 pA	−25 / 10 / 25 / 25 pA	−10 pA	−50 / 15 pA	−50 / −25 pA	−100 pA	−30 pA
doubles ea. +10°C	doubles ea. +10°C	doubles ea. +10°C	doubles ea. +10°C	doubles ea. +10°C	doubles ea. +10°C	doubles ea. +10°C
±1 pA/V	±1 pA/V	±5 pA/V	±1 pA/V	±4 pA/V	±5 pA/V	±3 pA/V
±1 pA	±1 pA	±1 pA	±1 pA	±2 pA	±2 pA	±1 pA
±0.3 / 0.1 / 0.1 pA	±10 / 5 / 10 / 10 pA	±2 pA	25 / 10 pA	±10 pA	±10 pA	±10 pA
10^{13} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{11} Ω ‖ 3 pF	10^{11} Ω ‖ 3 pF	10^{12} Ω ‖ 4 pF
10^{13} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 3 pF	10^{12} Ω ‖ 10 pF
0.5 µV	4 µV	5 µV	4 µV	8 µV	15 µV	6 µV
0.04 pA	0.5 pA	0.2 pA	0.5 pA	0.3 pA	0.1 pA	0.1 pA
2.9 µV	3 µV	2 µV	2 µV	3 µV	4 µV	2 µV
0.05 pA	0.5 pA	0.6 pA	0.5 pA	1 pA	2 pA	1 pA
5 µV	3 µV	4 µV	3 µV	4 µV	4 µV ④	2 µV
0.03 pA	0.2 pA	2 pA	0.2 pA	3 pA	5 pA	2 pA
±15 V(±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±12 to ±18 V)	±15 V (±10 to ±18 V)	±15 V (±4 to ±24 V)
±3 mA (±8 mA)	±2.8 mA (±7.8 mA)	±10 mA (±15 mA)	±2.8 mA (±7.8 mA)	±15 mA (±25 mA)	±10 mA (±32 mA)	±1.0 mA (±3.0 mA)
0 to +70	−25 to +85	0 to +70	−25 to +85	−25 to +85	−25 to +85	−25 to +85
−65 to +150	−65 to +150	−55 to +125	−65 to +150	−65 to +150	−55 to +125	−55 to +125
TO-99	TO-99	S4	TO-99	TO-8	S4	TO-8
*	*	*	*	USQ	*	US-Q

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.

Bipolar Microcircuits

← GENERAL PURPOSE → LOW VOLTAGE DRIFT ←→ WIDEBAND →

Specifications typical at 25 °C with nominal power supply, unless otherwise indicated.

			1339 General Purpose	133901	133902	1319 High Performance Low Drift	131901	1317 Wideband
OUTPUT RANGE	E_O	Voltage, min	±10 V			±10 V		±10 V
	I_O	Current, min	±5	10	10 mA	±5 mA		±10 mA
GAIN	A_O	dc open loop, rated load, min	15	40	50 k	50,000		20,000
FREQUENCY RESPONSE (Inverting)	f_t	Small signal (unity gain, open loop), min	100 MHz (typ.) ⓪			1 MHz (typ.)		70 MHz (typ.) ⑧
	f_p	full output (p-p), min	500 kHz (typ.) ①			8 kHz		60 kHz (typ.) ⑨
	s_r	Slew rate	34 V/μSec ①			0.6 V/μSec		5 V/μSec ⑨
	t_s	Settling time (0.1%)	--			--		--
INPUT VOLTAGE RANGE	E_{CM}	Common mode (dc linear operation), min	±11 V			±12 V		±7 V
		(fault), abs max	±15 V			±15 V		±15 V
	CMRR	Common mode rejection ratio (dc)	100,000			100,000		10,000
INPUT VOLTAGE OFFSET	E_{OS}	Initial (without ext. trim) @25 °C max	±7.5	7.5	3 mV	±5	2 mV	±10 mV
	R_{OS}	Zero adjustment	100 kΩ pot			10 kΩ rhst		25 kΩ pot
	$E_{OS}TC$	Vs. Temperature Range	±12	5	5 μV/°C	±5	±2 μV/°C	±5 μV/°C
	PSRR	Vs. Power Supply	30 μV/V			10 μV/V		±100 μV/V
INPUT BIAS CURRENT	I_B	Initial @ 25 °C, max	1000	600	500 nA	250	50 nA	+750 nA
	I_D	Offset (tracking)	20 nA			3	2 nA	±50 nA (max.)
	I_{DTC}	Offset vs. temperature range	±200 pA/°C			±30 pA/°C		±9 pA/°C
INPUT IMPEDANCE	Z_o	Differential	300 kΩ ‖ 3 pF			2 MΩ ‖ 4 pF		1 MΩ ‖ 3 pF
	Z_{CM}	Common mode	50 MΩ ‖ 10 pF			600 MΩ ‖ 4 pF		500 MΩ ‖ 10 pF
NOISE	e_n	Midband, voltage rms (10 Hz to 10 kHz)	2 μV			1 μV		1 μV
POWER REQUIREMENT	$\pm V_{CC}$	Nom. Supply Voltage (Voltage Range)	±15 V (±9 to ±18 V)			±15 V (±8 to ±22 V)		±15 V (±8 to ±22 V)
	$\pm I_{CC}$	Current: quiescent (full load), max	±7 mA (±12	17	17 mA)	±3 mA (±8 mA)		±4 mA (±14 mA)
TEMPERATURE RANGE (°C)	T_O	Operating	0 to 70	0 to 70	-55 to +125	0 to 70	-55 to +125	-55 to +125
	T_S	Storage	-65 to +150			-65 to +150		-65 to +150
MECHANICAL See pp., 62-69		Outline drawing	TO-99			TO-99		TO-99
		Socket	*			*		*

0. GBW @ A = 100
1. @ A = 100, 4.2 V/μSec @ A = 1
2. G x BW @ A = 10, f_t = 10 MHz @ A = 1 (typ.)
3. 3.5 μSec to 0.01%
4. G x BW @ A = 10
5. 3 μSec to 0.01%
6. 5 Hz to 50 kHz
7. When inputs are less than 5 mV apart. When inputs are more than 50 mV apart quiescent current is ±3 mA typical.
8. G x BW @ A = 100
9. @ A = 100
10. @ A = 5
11. R_1 = 220 Ω, C_1 = 22 pF, NOISE Gain = 1
12. Inverting or non-inverting
13. Noise Gain = 2, R_1 = 220 Ω, C_1 = 15 pF

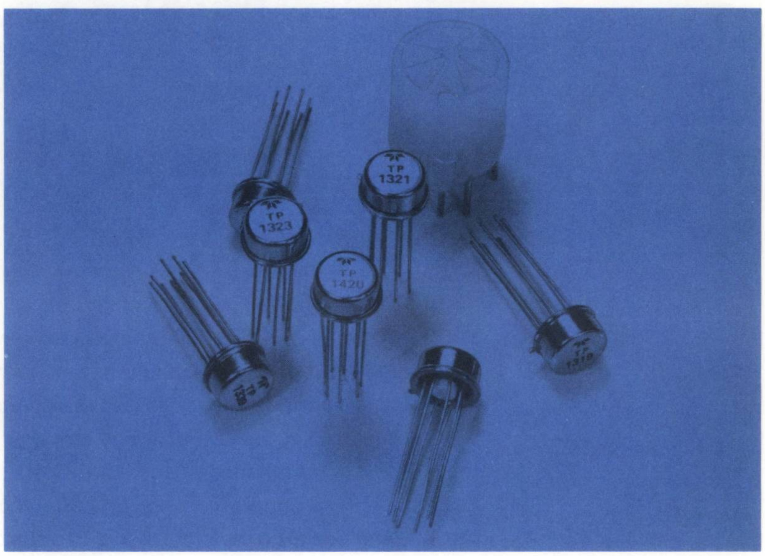
* Socket not supplied by Teledyne Philbrick

WIDEBAND → ← SPECIAL PURPOSE →

1321 132101 Wideband High Input Impedance		1322 132201 High Slew Rate		1324 132401 Fast Settling		1323 132301 132302 Low Power General Purpose		
±10 V		±10 V		±10 V		±12 V		
±10 mA		±10 mA		±10 mA		±10 mA		
80,000		7,500		100,000		200,000		
100 MHz (typ.) (3)		20 MHz (typ.) (4)		8 MHz (11) (12)		1 MHz (typ.)		
320 kHz (10)		1.2 MHz (10)		350 kHz (11) (12)		25 kHz (typ.)		
35 V/μSec (10)		120 V/μSec (10)		35 V/μSec (11) (12)		20 V/μSec		
500 nSec (3)		300 nSec (5)		1.0 μSec (12) (13)		10 μSec		
±12 V		±10 V		±10 V		±11 V		
±15 V		±15 V		±15 V		±15 V		
100,000		30,000		150,000		200,000		
±5 mV		±10 mV		±10	3 mV	±5	3	3 mV
100 kΩ pot		20 kΩ pot		50 kΩ pot		1 MΩ pot		
±20 μV/°C		±15 μV/°C		±30	15 μV/°C (max.)	±10 μV/°C		
30 μV/V		30 μV/V		10 μV/V		10 μV/V		
±25 nA		±250 nA		+300	200 nA	±40	20	20 nA
5 nA		20 nA		50	35 nA	2.5 nA		
0.8 nA/°C		±0.5 nA/°C		±0.3 nA/°C		0.5 nA/°C		
300 MΩ ∥ 3 pF		100 MΩ ∥ 3 pF		3 MΩ ∥ 3 pF		2 M ∥ 3 pF		
1000 MΩ ∥ 3 pF		1000 MΩ ∥ 3 pF		1000 MΩ ∥ 3 pF		200 M ∥ 3 pF		
1 μV		1 μV		6 μV		10 μV		
±15 V (±8 to ±22 V)		±15 V (±8 to ±20 V)		±15 V (±12 to ±18 V)		±15 V (±5.5 to ±20 V)		
±4 mA (±14 mA)		±6 mA (±16 mA)		±15 mA (±25 mA)		±80 μA (7)		
0 to 70	−55 to +125	0 to 70	−55 to +125	0 to 70		0 to 70	−25 to +85	−55 to +125
−65 to +150		−65 to +150		−65 to +125		−65 to +150		
TO-99		TO-99		TO-100		TO-99		
•		•		•		•		

Selected versions are available on all models, consult factory.

Specifications listed left to right correspond to model numbers top to bottom above.



Instrumentation Amplifiers

FEATURES

- Ultra High Z_{in} – 10^{13} Ω
- Very Low Drift – 1 μV/°C max.
- High CMRR – 116 dB min. to 100 Hz
- Low Noise – 2 μV p-p flicker
- Low Bias Current – 10 pA max.
- Single Resistor Gain Selection
- Sense Terminal for Current Feedback
- ±10 V Output Offsetting Capability
- Small Size, Low Profile – 2 x 2 x 0.4"

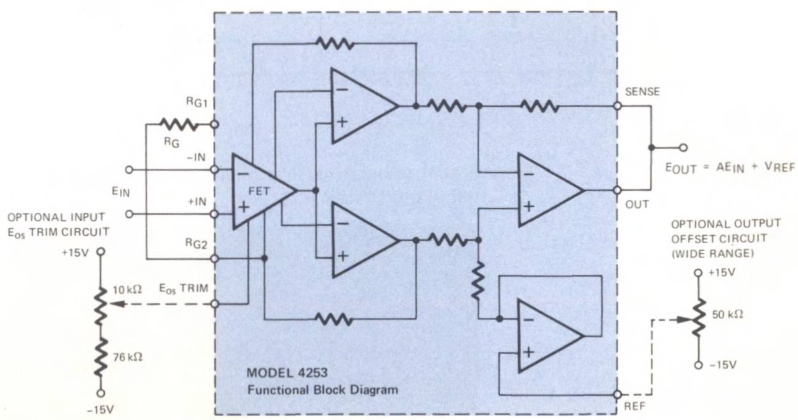
APPLICATIONS

- Low Level Instrumentation
- High Resolution Control Loops
- High Impedance Sensors
- Pressure Transducers
- Bridge Amplifiers
- Biomedical Engineering

MODELS 4253 and 425301

Philbrick's high-performance FET Instrumentation Amplifiers, Models 4253 and 425301, are specifically designed to extract and accurately amplify small differential signals from large common mode voltages. A unique bootstrapped FET input circuit provides a very high input impedance to minimize source-loading errors even from very high source impedances. Computer testing and matching of active devices plus the use of precision passive components ensures extreme stability with time and temperature, and provides very low input noise. Functional trimming is used during manufacture to guarantee excellent Common Mode Rejection for both ac and dc signals, even with large source unbalances.

The gain range is adjustable between 1 and 5000 by one external resistor, excellent linearity being maintained throughout this range. The circuit design also includes a provision for offsetting the output by up to ±10 volts, and features output short circuit protection. Reliable performance even in severe vibration environments is ensured by low profile epoxy encapsulation.



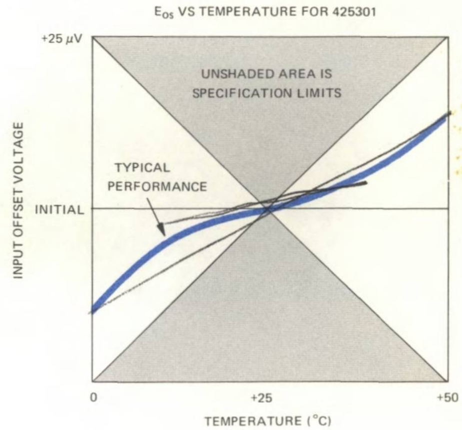
MODEL 4253
Functional Block Diagram

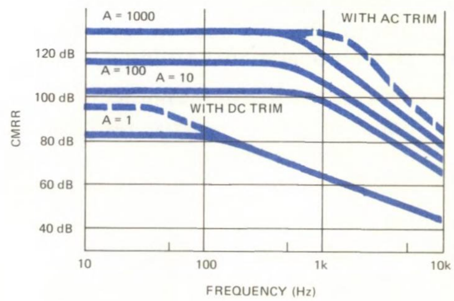
MODELS 4251 and 4252

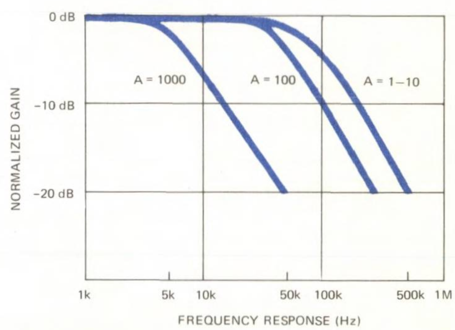
These instrumentation amplifiers feature extended frequency response and a gain range of 1 to 1000 programmable with a single resistor. Offset voltage is externally adjustable to zero. An output sense terminal allows the amplifier feedback to be taken precisely at the load point. A-Another feature is the CMRR adjust terminal, which allows external trimming of the common mode rejection ratio at the exact gain and frequency desired. This terminal also serves as a reference point for the amplifier output, and output offsets of up to ±10 volts can be introduced.

	4251 4252 Wideband Bipolar	4253 425301 Low-Drift FET
GAIN		
Gain Range (Adj. with Ext. Res.)	1–1000	1–5000
Gain Programming	$A = 1 + \frac{20\ k\Omega}{R}$	$1 + \frac{100\ k\Omega}{R_G}$
Gain dc Nonlinearity, Max.	±0.01%	±0.005%
Gain dc Nonlinearity vs. Temp. (A = 100)	10 ppm/°C	30 ppm/°C
INPUT CHARACTERISTICS		
Input Impedance – Differential	50 MΩ	10^{13} Ω
Input Impedance – Com. Mode Min.	30 MΩ	10^{13} Ω
Input Voltage Range, Min.	±10 V	±10 V
OFFSETS AND NOISE		
Input Offset Voltage (RTI) Gain = 1000	±3 mV	±1 mV
Input Voltage Offset 425301	—	500 µV
Input Voltage Offset vs. Temp. G = 1000	±2 µV/°C	±2 µV/°C
Input Voltage Offset vs. Temp. 425301	—	±1 µV/°C
Input Bias Current	30 nA	-10 pA
Input Bias Current vs. Temp., Max.	±3 nA/°C	2 x 10°C
COMMON MODE REJECTION (dc–100 Hz)		
A = 10, Balanced Source, Min.	80 dB	82 dB
A = 10, Balanced Source, Min. 425301	—	92 dB
A = 1000, Balanced Source	110 dB	114 dB
A = 1000, Balanced Source 425301		120 dB
FREQUENCY RESPONSE		
Small Signal A = 100, ±1% Accuracy, Min.	25 kHz	500 Hz
OUTPUT CHARACTERISTICS		
Rated Output Voltage, Min.	±10 V	±10 V
Rated Output Current, Min. 4251	±100 mA	±5 mA
Rated Output Current, Min. 4252	±5 mA	—
POWER SUPPLY REQUIREMENTS		
Supply Voltage, Rated	±15 V	±15 V
Supply Current, Quiescent, Max.	±15 mA	±16 mA
TEMPERATURE RANGE (Degrees C)		
Operating, Rated Specs	-25 to +85	0 to +50
Storage	-55 to +100	-55 to +125

Typical performance curves for 4253 Series.





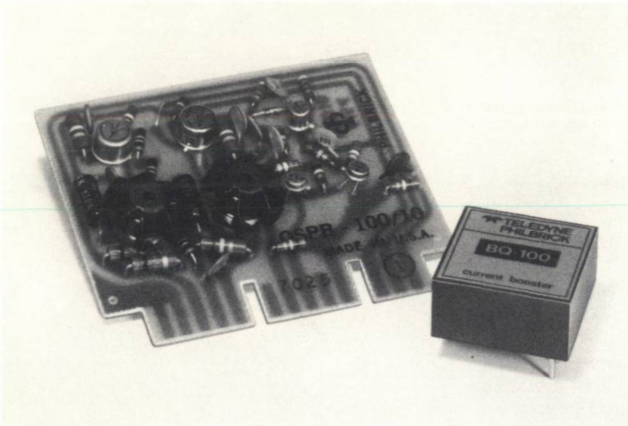


APPLICATION NOTE:

Recommended grounding and shielding practices for instrumentation amplifiers:

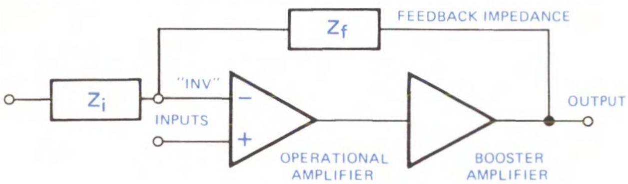
a. Ensure that the data acquisition system has a stable ground.
b. Ground the signal circuit at one point only.
c. Signal cable shields should not be used to carry signal currents; they should be connected to ground at only one point, preferably at the signal source.
d. If the signal source operates off ground at some common mode voltage, the signal cable shield should not be grounded; it should be connected to the center-tap or the "low" side of the signal source.

Booster Amplifiers

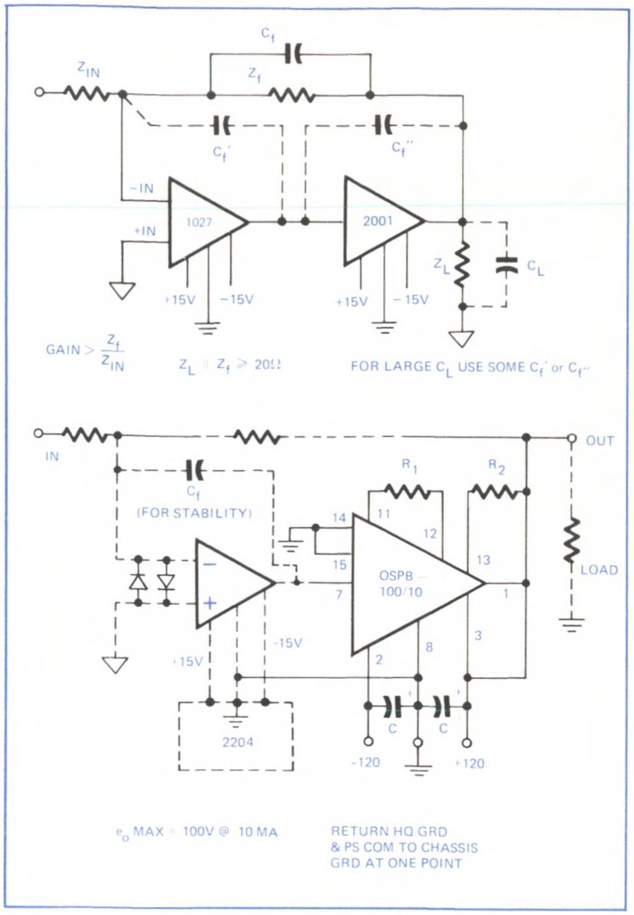


By definition, a Booster is a power amplifier. A current booster is used when the output current is too small to drive the necessary load. Voltage boosters are also available to extend output voltage capabilities of the standard 10 Volt operational amplifier. (See OSPB-100/10)

Because the booster is normally connected inside the operational amplifier's negative feedback loop, its contribution to drift, linearity, and gain error is negligible.



NOTE: If voltage booster is used, do not exceed common mode voltage capability of the amplifier.



		BQ-100	2001	OSPB-100/10
OUTPUT	Voltage, min.	±10 V	±10 V	±100 V
	Current, min.	100 mA	500 mA	1.5 mA (10 mA)*
VOLTAGE GAIN (DC open loop)	At rated load, min.	0.95	0.90	19
	Current gain, min.	2000	40,000	
FREQUENCY RESPONSE	Full output (no distort.) min.	400 kHz	80 kHz	10 kHz
	Rate limit	35 V/μSec	10 V/μSec	7 V/μSec
INPUT VOLTAGE OFFSET	Initial @ 25°C	±0.3 V	±0.3 V	±0.1 V
INPUT IMPEDANCE	Pos. or neg. input to common	600 kΩ	1 MΩ	1 MΩ
OUTPUT IMPEDANCE	Output to common	3 Ω	1 Ω	500 Ω
POWER REQUIREMENTS	Nominal supply voltage	±15 V	±15 V	±120 V
	Voltage range	±12 to ±16 V	±12 to ±16 V	±100 to ±125 V
	Current (quiescent), max.	±15 mA	±50 mA	±3.5 mA
	(full load), max.	±120 mA	±550 mA	±6 mA (±15 mA)*
	Operating	−25 to +85	−25 to +65	−25 to +85
	Storage	−55 to +100	−55 to +100	−55 to +85
CASE STYLE & SOCKET		AS2, NSK-20	G1, NSK-9	SP, QS-15

*Specifications shown in parenthesis apply when external boost resistors are used. See OSPB-100/10 data sheet.

Operational Manifold

Teledyne Philbrick Model 5001 Operational Manifold provides the capability of simulating small analog systems and performing computations using plug-in Function Boards that accept many types of operational amplifiers as well as linear and non-linear function modules. The Model 5001's versatility proves invaluable for applications requiring varied types of computing elements.

In addition to its dynamic breadboard characteristics, the Model 5001 is an outstanding educational tool for learning analog theory and circuit design from the basics through complex analog computation and control.

Each Function Board provides a socket for the active operator, and a logical patch field for connecting active and passive elements and interfacing associated circuitry.

The patch field greatly reduces breadboarding time normally required for testing applications. When used for teaching purposes the patch field makes a lucid, easy-to-follow circuit.

The Model 5001 incorporates a built-in regulated dual power supply. The regulated voltages are brought out to Function Board jacks for use as input or reference voltages.

Circuit wiring and interface is performed using standard banana plug patch cables, shorting bars, and plug-in passive and active elements. External signals and output indicators are connected in the same manner.

The Model 5001 is available as a bench model or in a standard, 19 inch rack model. A complete line of accessories is available which includes a variety of Function Boards, hardware kits, and component kits.

ACCESSORIES

MODEL 6048 FUNCTION BOARDS

This Function Board accepts the standard 7 or 9 pin "Q" package operational amplifiers. The patch field for interconnecting operational elements includes jacks for external trim, ±15 Vdc regulated, signal ground and power ground.

MODEL 6042 FUNCTION BOARD

This Function Board accepts integrated circuit operational amplifiers similar to 709's or 741's in TO-99 packages.

The patch field includes jacks for external trim, damping networks, ±15 Vdc regulated, signal grounds and power ground.

MODEL 6049 FUNCTION BOARD

This version accepts our Model 4850 Three-Mode Integrator. Model 6049 is a double size board and comes supplied with the Model 4850. See pages 58 and 59 for specifications on Model 4850.

MODEL 6054 FUNCTION BOARD

This Function Board accepts Philbrick Models 4350 and 4351 Log Modules and provides an output proportional to the log or antilog of the input signal. Either a Model 4350 or 4351 is supplied with this double-size function board (specify). See page 52 for 4350/4351 specifications.

MODEL MAK–2F CONNECTION HARDWARE KIT

The MAK–2F Hardware Kit includes

- 4 shielded twin tip cables,
- 12 single tip patch cords,
- 32 twin tip plugs (for component mounting) and
- 15 twin tip shorting plugs

MODEL CCK–MF COMPUTING COMPONENT KIT

The CCK–MF Kit includes the following components mounted on twin tip banana plugs.

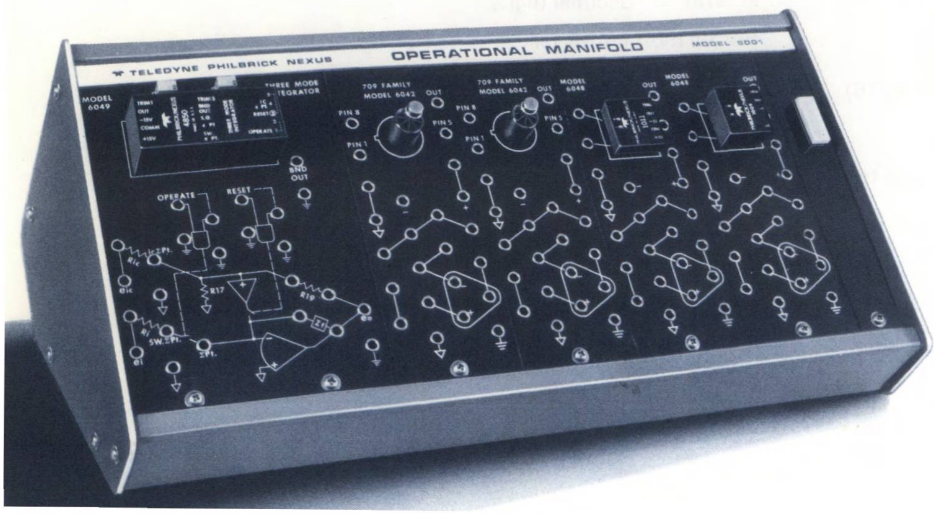
- 4 Diodes 1N914
- 2 Zener Diodes 9.5 V, 5%
- 40 resistors, and
- 12 capacitors

SPECIFICATIONS

INPUT VOLTAGE	115 V ±10% (5001) 230 V ±10% (5001-01) 50–400 Hz
POWER SUPPLY	
Output Voltage	±15 (±0.15) Vdc
Output Current	±100 mA min.
Regulation to line	±0.03% max.
Regulation to load	±0.03% max.
Ripple and Noise	1.0 mV rms

Complete protection against shorts for an indefinite period.

DIMENSIONS	17"L x 12"W x 7.75"H
WEIGHT	6 lbs (without Function Boards)
NO. CHANNELS	6 single boards or 3 double boards



ORDERING INFORMATION

Model 5001 (specify bench or rack model) (5001-01 for 230 V) (Does not include function boards. Order separately as listed below).

Model 6042 Function Board (less operator)

Model 6048 Function Board (less operator)

Model 6049 Function Board (Model 4850 Three Mode Integrator supplied)

Model 6054 Function Board (Model 4350 or 4351 Log Module supplied – please specify)

MAK–2F Connection Hardware Kit

CCK–MF Computing Component Kit

DATA CONVERSION PRODUCTS

Philbrick manufactures a comprehensive line of data conversion products with an outstanding range of performance characteristics. Reinforced by the reliability, quality, and experienced applications support you expect from Philbrick, these data conversion products are ideally suited for optimizing future designs or upgrading present ones.

ANALOG/DIGITAL CONVERTERS

Philbrick A/D Converters are self-contained, low-profile modules utilizing integration, modified successive approximation, or tracking circuit techniques to provide the right price/performance combination for a wide variety of applications. Proprietary design techniques and the use of high quality components assure adjustment-free operation over the operating temperature range. A feature of Philbrick A/D's allows the user to select single (from external command) or repetitive operation for digital display. Other key features include . . . .

- 10 μSec conversion time for 12-bits (4106)
- Excellent PSRR to ±0.001%/%ΔVs
- Relative accuracy ±½ LSB maximum (±¼ LSB max. model 4110)
- BCD output (models 4111 and 411110)
- DTL/TTL compatible
- Continuous Tracking and converting (model 4110)

DIGITAL/ANALOG CONVERTERS

Philbrick D/A converter modules are self-contained, low-profile units accepting 8 to 14-bit digital inputs and providing either a voltage or current output. With built-in reference, high speed switching, and a fast settling amplifier in voltage models, each amplifier is fully specified to minimize application difficulties and designed for long-term accuracy and reliability.

- Linearity ±¼ LSB , typical (±¼ LSB max. on 4050 Series)
- DTL/TTL compatible
- Buffered inputs on high performance models
- 100 ns Settling Time to 0.01% (models 4014, 4016)
- Excellent PSRR to ±0.002%/%ΔVs
- Low Cost: $19 (1–9 qty. models 4020, 4021)
- Microcircuit - Hermetically sealed manufactured to MIL-STD-883 (4050 Series)
- Multiplying (models 4028 and 4029)

D/A Converters used in display systems, control systems, and other demanding applications must have good accuracy and resolution; slew and settle quickly; exhibit a high degree of linearity; have extremely low noise and no glitches. For such requirements Philbrick offers the models 4015, 4017, and 4002. Each is actually a small system within a card-mounted module utilizing a unique current-stabilized, non-saturating switching concept to preserve linearity and stability at high speed and eliminate switching transients.

If high performance over a wide temperature range is needed, the 4050 Series of microcircuit D/A Converters is recommended. These units are packaged in a hermetically sealed double D.I.P. and can be processed to MIL-STD-883 to ensure high reliability in military or rugged industrial applications.

A key data conversion accessory is Philbrick's new model 4853, a high-speed sample-hold amplifier for precision applications. This sophisticated module is particularly well suited for use with A/D Converters (particularly successive approximation) and multiplexers in high through-put 12-bit data-acquisition systems.

A new monolithic quad current switch, Model 3420, is also featured in this section. Philbrick has combined a special topographical design with high quality PNP transistors to achieve higher speeds and greater accuracy than previously possible. Use the Model 3420 to design higher performance D/A and A/D Converters at lower cost.

D/A & A/D PARAMETER DEFINITIONS

RESOLUTION: The relative value of the Least Significant Bit (LSB) - the smallest value of change that can be distinguished by an A/D Converter or generated by a D/A Converter. Resolution is determined by Full Scale/2^n for a converter with "n" binary bits or Full Scale/10^d for a BCD Converter with "d" decimal digits.

For an n-bit converter

A.) Number of steps:

1.) Binary: $2^n - 1$

2.) BCD : $10^d - 1$

B.) Value of Smallest step (LSB)

LSB = Full Scale/2^n

C.) MSB (most significant bit) = Full Scale/2

D.) Full Scale is unreachable by 1 LSB

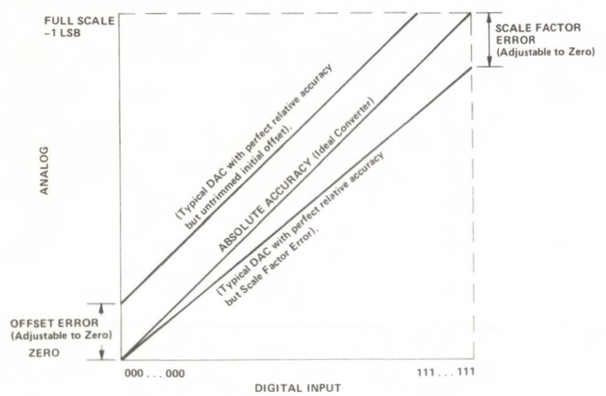
For example, a 12-bit converter has an LSB of 0.0244% of Full Scale. With a Full Scale voltage of 10 V the maximum output voltage is 10.00000 V –0.00244 V or 9.99756 V.

ABSOLUTE ACCURACY: Absolute accuracy for a Converter is defined as the degree to which the actual input-output relationship matches the ideal calculated relationship.

RELATIVE ACCURACY: The relative accuracy of a converter is determined by its linearity, and does not include its Scale Factor (gain) and Offset errors. After its Gain and Offset errors are adjusted, a converter with perfect relative accuracy will display perfect absolute accuracy.

SCALE FACTOR ERROR (GAIN ERROR): The difference in slope between the actual input-output relationship and the ideal relationship. This is quoted in percent error of value, ignoring offset error. Normally, this error is easily adjusted out in system calibration.

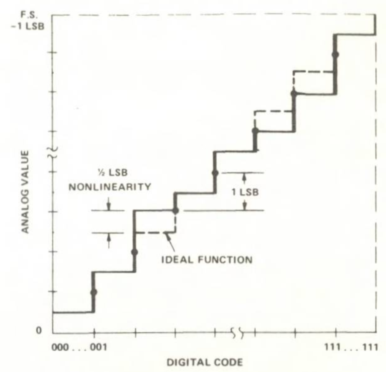
OFFSET ERROR: The degree to which the transfer function fails to pass through the origin normally measured on the analog axis. If this error is not adjusted to zero, a constant absolute accuracy error is obtained at every point on the transfer function. Offset error does not degrade the relative accuracy.



SCALE FACTOR & OFFSET ERROR

ADC OFFSET MEASUREMENT: Because of quantization the actual offset of an ADC cannot be measured directly and must be calculated from another measurement or set of measurements. Normally, to plot the transfer function of an ADC, we would measure the analog inputs that result in transitions on the digital output. Since the first transition would ideally occur at +½ LSB, the discrepancy of this first transition is sometimes considered to be the offset error. Each transition, however, is permitted to have offset, scale factor, and linearity errors. Thus another way to measure ADC offset is to extrapolate to zero the best straight line drawn through several lower transitions.

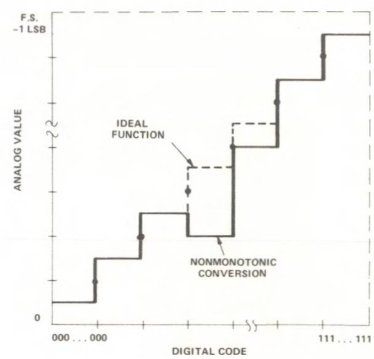
NONLINEARITY: Nonlinearity is the maximum deviation from a straight line drawn between the end points of the input/output transfer function. Nonlinearity is normally specified as some fraction of an LSB. For example, a specification ±½ LSB requires the sum of either the positive errors or the negative errors of the individual bits not to exceed ½ LSB.



DIFFERENTIAL NONLINEARITY

DIFFERENTIAL NONLINEARITY: Differential Nonlinearity describes the difference between the actual analog transition and the calculated value of the LSB over the full digital range. For example, differential nonlinearity of ±½ LSB demands that each step be 1 LSB ±½ LSB. A differential nonlinearity of ⩽1 LSB is the maximum allowed for monotonic operation.

MONOTONICITY: A converter is monotonic when it is continuously increasing in response, and each successive level is equal to or greater than the previous one. Monotonicity requires differential nonlinearity to be ⩽1 LSB.

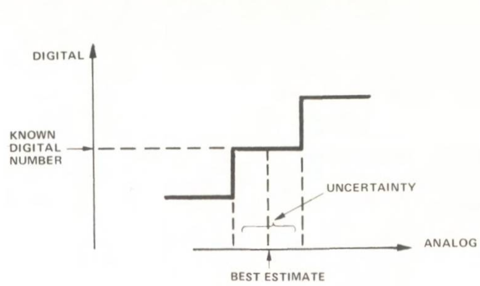


NONMONOTONIC TRANSFER FUNCTION

QUANTIZING ERROR: The inherent uncertainty of ±½ LSB associated with the finite resolution of the digitizing process in ADC's. This uncertainty is the finite scientific rounding to whole LSB's and will occur as an uncorrectable uncertainty even in ADC's with perfect absolute accuracy.

With reference to the drawing shown below, if the digital word is known, the analog input that generated it can only be established with a ±½ LSB uncertainty.

In the measurement of ADC's, Quantization Error can be eliminated by monitoring transition points.



QUANTIZING ERROR

POWER SUPPLY SENSITIVITY: Most converter specifications are defined at the nominal power supply voltages. Depatures from these specifications will occur at other supply voltages and are usually specified as a worst case degradation per percent change in the power supply voltage. Normally quoted are:

Sensitivity of scale factor to power supply variation
Sensitivity of offset to power supply variation

NOTE: Differential Linearity is normally not significantly affected by variations in power supply voltage.

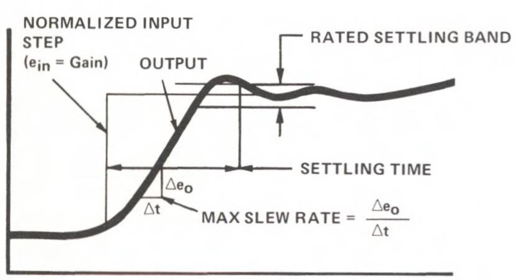
STABILITY: Variations in converter performance due to the passage of time. Converters designed for superior time stability are built with aged components including wire-wound resistors. Philbrick recommends product burn-in and temperature cycling for applications requiring the ultimate in stability.

ANALOG NONLINEARITY (MDAC ONLY): The percentage deviation from the best straight line for the analog input to analog output transfer function.

FEEDTHROUGH (MDAC ONLY): The amount of analog output for various input frequencies with the digital word programmed for zero output.

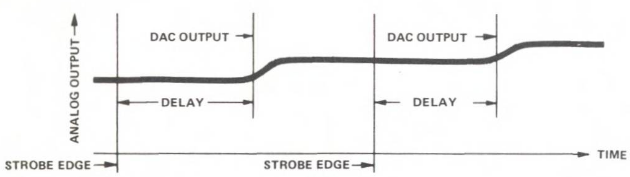
SETTLING TIME - DAC: Settling time for a DAC is the total time necessary for the DAC to complete a full-scale step (including switching, slewing, and small-signal settling) to within a defined error band at the output (normally ±½ LSB).

NOTE: Current output DAC's often settle very fast only with a low impedance load. Therefore, the specified settling time may not be attainable in many real system applications, without special circuitry.



DAC SETTING TIME

DAC DELAY: Deglitched DAC's have a built-in time delay (often variable by external control). This parameter defines the time delay between the strobe leading edge and initiation of the output voltage change, and does not include settling of the output.



DELAY TIME IN DEGLITCHED DAC's

SLEW RATE: The maximum rate at which a DAC output voltage can change in response to a full-scale-output command. Slew rate is only a guide to speed. In most applications, the important specification is the settling time, which is speed to rated accuracy.

CONVERSION TIME: Time required to reach the computed output by an ADC. In successive-approximation converters the conversion time is independent of input amplitude (ranging from 1 μSec to 200 μSec). In integrating converters the conversion time is somewhat proportional to the input amplitude, varying about 50% from zero to full scale (ranging from 1 ms to desired noise-eliminating, integrating period). Conversion time for a tracking converter is very fast for small signals (100 ns per LSB step change, for example), but will be much longer for large signal charges.

DAC - MAXIMUM WORD RATE: This parameter, (which has many names, e.g. throughput rate, etc.) defines the maximum rate at which a DAC may be commanded to make 1 LSB steps. The Word Rate is necessary to understand the DAC's limitations when driving it from a counter to generate analog ramps.

ADC UPDATE RATE: This is the maximum cyclical rate at which the ADC may make repetitive conversions.

NOTE: This is not necessarily equal to the reciprocal of the conversion time, as many converters require time to reset before initiation of the next conversion. Also, in buffered ADC's there must be a time allowance for input settling. The digital output is normally held for at least 1 clock pulse after conversion.

SETTLING TIME - ADC: Settling time for an ADC is the time required after a full scale input change before a conversion may be initiated.

NOTE: Amplified-input ADC's will be slower in this regard because of settling of the input amplifier.

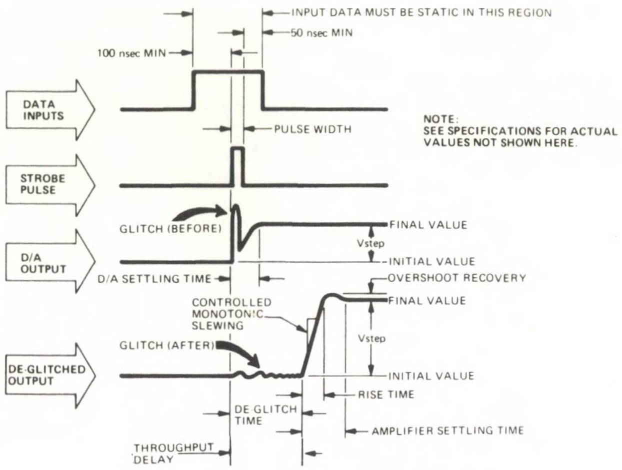
GLITCH: A glitch or transient spike occurs in all DAC's when it changes from one level to another. The glitch is caused by the skewing of analog switches (switches turning on faster than off, or vice versa) and is most pronounced for small changes around the MSB.

NOTES ON GLITCHES

1.) Glitches in standard DAC's, when measured with infinite bandwidth, may display amplitude peak = Full Scale/2. The pulse width of the glitch will depend upon the skew of the input data as well as the DAC's design. The true measure of the glitch is not its amplitude, but its area (integral) in volt-seconds which is normally unaffected by the bandwidth of the system. The glitch peak amplitude amy be reduced arbitrarily by filtering of the DAC output.
2.) The glitch is often produced when a DAC is fed high-skew words.
3.) A well-designed standard DAC with F.S. = 10 volts when driven from TTL registers can be expected to have a major transition glitch of less than 200×10^{-9} volt-seconds.
4.) Deglitched DAC's often have two glitch specifications:
    a.) The area magnitude of the repetitive glitch, i.e. the glitch that occurs for every transition. This

can often be treated as an offset voltage.

b.) The maximum change in glitch area magnitude as a function of changes in the digital word. This must be considered as equivalent to a dynamic linearity error and when generating a ramp, may not be discernable from a differential nonlinearity error.



TIMING DIAGRAM OF DEGLITCHED DAC

TEMPERATURE PERFORMANCE: In addition to the performance at +25 °C specified for a converter, there usually are quoted certain temperature coefficients which define the expected performance degradation per degree departure from the specified temperature. Those most commonly quoted per:

1.) SCALE-FACTOR TEMPERATURE COEFFICIENT: The slope deviation caused by bit weighting resistor ratios, terminating resistor and reference circuitry not tracking perfectly with temperature. The total scale factor change is specified in ppm/°C of reading.

2.) OFFSET TEMPERATURE COEFFICIENT: The overall converter drift with temperature. Caused by switch leakages, output amplifier offset T.C. (voltage DAC's), and buffer amplifier and comparator T.C. (ADC's). Bipolar Offset Temperature Coefficient, for offset binary, is affected mainly by the tracking of the offsetting resistor to the MSB with temperature. Offset Temperature Coefficient is expressed in ppm/°C of full scale.

3.) LINEARITY TEMPERATURE COEFFICIENT

4.) DIFFERENTIAL NONLINEARITY TEMPERATURE COEFFICIENT: Describes the tracking of the bit weights to each other. A converter may have acceptable differential nonlinearity at 25 °C, but at some other temperature it may be greater than 1 LSB, causing the converter to be non-monotonic.

STATIC ERROR ANALYSIS: In any given application the various sources of error must be properly accounted to determine expected system performance. This analysis must be tailored to the specific application. In many applications, for example, differential linearity is important while overall linearity is less important. Other applications are very forgiving of offset and/or scale factor errors.

In the more extreme cases where full absolute accuracy of the transfer function is required, all sources of error must be added for the worst-case condition to be established.

Example: 12-Bit D to A Converter
Assume Scale Factor error and Offset errors are trimmed to zero at 25 °C, $\Delta T = 50\,°C$, $\Delta Vcc = \pm 1\%$

Nonlinearity ±0.5 LSB
Noise ±0.1 LSB

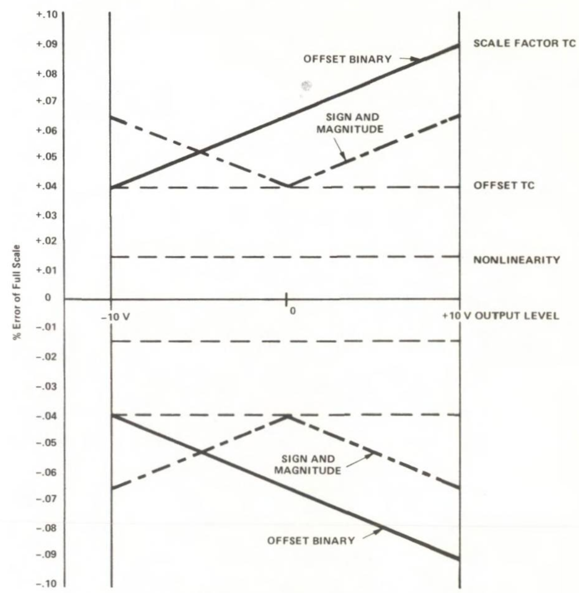
$\pm 0.6\ LSB = 1/2^{12} \times 0.6 = \pm 0.000146$ of F.S.

Scale Factor ±10 ppm/°C = 0.00001 of value/°C. For 50 °C = ±0.0005 of value.

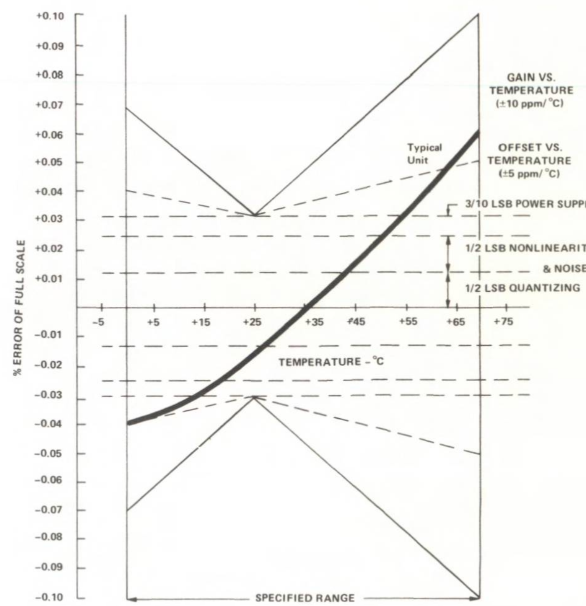
Offset ±5 ppm/°C = ±0.000005 of F.S./°C. For 50 °C = ±0.00025 of F.S.

Power Supply Sensitivity ±0.002%/%Δ Power Supply. For ±1% = ±0.00002 of value.

Max. Total Error = (±0.000146 ±0.0005 ±0.00025 ±0.00002) × F.S. = (0.000916 × F.S.)
(for all conditions at full scale)



OFFSET BINARY AND SIGN & MAGNITUDE AT TEMPERATURE EXTREMES



ABSOLUTE WORST CASE ERROR BAND FOR A/D CONVERTER – 12 BITS
(Gain T.C. ±10 ppm/°C & OFFSET T.C. = ±5 ppm/°C)

ANALYSIS OF DIFFERENTIAL NONLINEARITY VS. TEMPERATURE: The preceding analyses have shown the absolute worst-case errors vs. temperature and power supply, but tell nothing about the differential nonlinearity of the converter. For example, over what temperature range will the converter be monotonic?

Since monotonicity requires differential nonlinearity $\leqslant$1 LSB, a converter with an initial differential nonlinearity of ±½ LSB at 25°C must have a T.C. $\leqslant$½ LSB/ΔT to maintain monotonicity. Thus, in a 12-bit converter (where ½ LSB = 122 ppm of F.S.), monotonicity over a ±50°C variation in the worst case requires a differential nonlinearity

$$\text{T.C.} = \frac{122\ \text{ppm}}{50\,^\circ\text{C}} = 2.44\ \text{ppm}/^\circ\text{C of F.S., max.}$$

SAMPLE-HOLD PARAMETER DEFINITIONS

The definitions which Philbrick applies to the key parameters of the 4853 are listed below. To minimize confusion, these definitions are essentially identical to those currently used by other large manufacturers of sample-hold amplifiers.

ACQUISITION TIME: The length of time between the Sample command and the moment the output is tracked to within the specified accuracy.

APERTURE TIME: The apparent time elapsed between the Hold command and the effective opening of the Hold switch. Sometimes referred to as "Turn-off Time".

IMPORTANT NOTE: Some manufacturers use the term aperture time when they are actually referring to aperture uncertainty time. As seen below, these are two completely different specifications.

APERTURE UNCERTAINTY TIME: The tolerance of the delay between a hold command and the actual opening of the hold switch. The variation of the aperture time.

BANDWIDTH: The frequency range over which the unit will operate within the rated accuracy. Although frequencies somewhat higher than this can be applied, the distortion and phase shift encountered may render inaccurate results.

DECAY RATE: The drift encountered when in the Hold mode.

FEEDTHROUGH: The effect of the input signal on the output when the amplifier is in the Hold mode. Usually a function of input signal level and frequency.

GAIN ERROR: The variation from nominal gain caused by component tolerances within the sample-hold amplifier.

GAIN T.C.: The effect that changes in ambient temperature have on the initial gain.

SWITCHING TRANSIENT: Voltage spikes generated when switching to Hold or Sample mode.

HOLD JUMP VOLTAGE: The output voltage step encountered when switching into the Hold mode, caused by a charge transferred to the holding circuit from the switch circuitry.

HOLD OFFSET VOLTAGE: The error voltage encountered when in Hold. This is a dc level that can have either a positive or negative value. It is composed of the Hold Jump Voltage and the Sample Offset Voltage.

SAMPLE OFFSET VOLTAGE: An error voltage encountered in the Sample mode which is due basically to the offset voltage of the internal op-amp. This dc level can have either a negative or a positive value and is one of the components of the Hold Offset Voltage.

APPLYING DATA CONVERTERS:

The following pages present the specifications for our data conversion products. The selection of the best converter for the job can be simplified by using the following outline as a guide:

D/A Converters Applications Notes

Current Output Models Why use one?

1.) For speed - They can be very fast with a low impedance load. In many cases a high speed operational amplifier is used on the output to achieve faster settling times for a desired voltage output. The ability to select the output amplifier permits circuit "tailoring" for economy and performance.
2.) For voltage scaling - By having a selectable gain operational amplifier on the output you can select the exact scale factor for the application. This method of adjusting the scale factor is far superior to that of varying the reference for a multiplying D/A, in terms of linearity.
3.) Driving a terminated line - Line losses will not affect output voltage
4.) Driving a comparator in A/D converters.
5.) Driving an active nonlinear network. Often devices such as logarithmic elements require a current input for maximum performance.
6.) For a power output - A current D/A can be fed directly into a current-to-voltage converter. Using a voltage DAC would put the errors of two amplifiers (and the additional cost) into the system.
7.) For signal multiplexing - Current switching is much faster and accurate than voltage switching.
8.) For driving an analog integrator - For applications such as a digitally controlled timer, a current output D/A interfaces directly with an integrator.

MULTIPLYING D/A's - IMPORTANT APPLICATIONS

1.) Display Systems
2.) Polar to Cartesian Coordinate Conversion
3.) Square law D/A or A/D conversion
4.) Precision low level multiplier
5.) Circuit linearity correction (Pincushion correction)
6.) Ratio taking A/D
7.) Digital-to-Analog converter

TYPES OF A/D CONVERTERS

SUCCESSIVE APPROXIMATION (S.A.) CONVERTERS

FEATURES:

A.) Very fast conversion per bit - even for purely random inputs.
B.) High resolution if desired
C.) Serial output and parallel output
D.) Overall Linearity is good
E.) Answer not dependent upon clock rate

CONSIDERATIONS:

A.) Signal must not change during the conversion time. Therefore, for many applications the S.A. converter must be preceded by sample and hold. Will not provide average over conversion period.

B.) Differential linearity only fair.

APPLICATION:

Successive approximation ADC's are most useful for data acquisition systems in conjunction with a multiplexer and high speed sample/hold amplifier. Excellent choice wherever high speed and accuracy are primary considerations.

INTEGRATING A/D CONVERTER

FEATURES:

A.) Excellent differential linearity

B.) No sample and hold required for most applications as output will be the average of the input during conversion period.

C.) Modest cost due to internal simplicity.

D.) By using an additional remote counter, single wire data transmission can be obtained.

E.) Answer independent of clock rate and capacitor value in two-slope unit.

F.) Good noise rejection.

CONSIDERATIONS:

A.) This conversion technique is generally slow.

B.) No true serial output is available.

C.) Unipolar only.

APPLICATION:

The integrating ADC is highly recommended for most applications where high speed is not a requirement. Applications such as digital voltmeters and digital weighing systems take advantage of the noise rejection and differential linearity features of integrating-type ADC's.

TRACKING CONVERTER

FEATURES:

A.) No sample and hold required.

B.) Output answer always valid.

C.) Equivalent update rate of 1 clock pulse for continuous signals.

CONSIDERATIONS:

A.) Quantization error ±1 LSB due to loop hysteresis.

B.) Long conversion time for large signal changes. (Typically 100 to 200 μSec).

C.) No serial output.

APPLICATION:

Tracking ADC's provide very fast conversion at low cost for applications such as process or servo control systems where the input signal is continuous and one converter can be used per signal input. Other applications include time expansion, transducer, and audio digitizing, and infinite track/hold amplifiers.

ANALOG TO DIGITAL CONVERTER COMPARISON

A TO D SPECIFICATIONS	A TO D TYPES		
	INTEGRATING	TRACKING	SUCCESSIVE APPROXIMATION
RESOLUTION & ACCURACY	Medium to High 8 to 16 Bits	Low to Medium 6 to 10 Bits	Medium to High 8 to 16 Bits
LINEARITY	±½ LSB to ±1 Count	±½ LSB or better	±½ LSB
CONVERSION TIME	.5 to 10 mSec SLOW	6 to 200 μSec but will change an LSB in 0.1 μSec. Very Fast per LSB	1 to 200 μSec Medium to Fast
COST	$50 to $200	$50 to $200	$50 to $1,000
OUTPUT	Parallel but count available for Serial	Parallel	Parallel & Serial
ADVANTAGES & DISADVANTAGES	Best Differential Linearity Least cost/Bit for many Bits High noise rejection SLOW, UNIPOLAR	Follows Input Min. cost/μSec for one input No latches required No serial output	Serial out standard versatile good cost/speed
TYPICAL APPLICATIONS	DVM's Weighing systems	Digitize voice & ∞ time sample & hold. Time expansion	Data Acquisition. General usage.
PHILBRICK MODELS	4109, 4109/10, 4111, 4111/10	4110	4103, 4104, 4105, 4106, 4107, 4108, 4112, 4113, 4114

Digital/Analog Converters

	Model	Resolution	Input Code Options (T^2L/DTL Compatible)	Output Options	Output Impedance (Unipolar/Bipolar)	Settling Time to % of F.S.
General Purpose Economy	4020	8-bits	BIN; OBIN	0 to +2 mA; −1 to +1 mA	8 kΩ/3.5 kΩ	300 ns to 0.05%
	4021			0 to −10 V; +5 to −5 V	<0.3 Ω	25 μs to 0.05%
	4022	10-bits	BIN; OBIN	0 to +2 mA; −1 to +1 mA	8 kΩ/3.5 kΩ	300 ns to 0.05%
	4023			0 to −10 V; +5 to −5 V	<0.3 Ω	25 ns to 0.05%
	4024	12-bits	BIN; OBIN	0 to +2 mA; −1 to +1 mA	8 kΩ/3.5 kΩ	300 ns to 0.01%
	4025			0 to −10 V; +5 to −5 V	<0.3 Ω	5 μs to 0.01%
	4026	12-bits	BCD	0 to +1.25 mA	5 kΩ	300 ns to 0.01%
	4027			0 to −10 V	<0.3 Ω	5 μs to 0.01%
General Purpose High Performance	4010	10-bits	BIN; OBIN	0 to +2 mA; −1 to +1 mA	8 kΩ/3.5 kΩ	300 ns to 0.01%
	4011		OBIN	+10 to −10 V	<0.3 Ω	5 μs to 0.01%
	4004	12-bits	BIN; OBIN	0 to +2 mA; −1 to +1 mA	8 kΩ/3.5 kΩ	300 ns to 0.01%
	4005		OBIN	+10 to −10 V	<0.3 Ω	5 μs to 0.01%
	4008	12-bits	BCD	0 to +1.25 mA	5 kΩ	300 ns to 0.01%
	4009			0 to −10 V	<0.3 Ω	5 μs to 0.01%
Ultra Fast	4014	12-bits	BIN; OBIN	0 to +16 mA; −8 to +8 mA	500 kΩ min.	100 ns to 0.01%
	4016	13-bits				
MIL-Grade Microcircuits	4050	8-bits	BIN; OBIN	0 to +3.2 mA; −1.6 to +1.6 mA	>3 kΩ	0.1 μs to 0.05%
	4051			0 to −10 V; +5 to −5 V [11]	>0.3 Ω	1 μs to 0.05%
	4052	10-bits	BIN; OBIN	0 to +3.2 mA; +1.6 to −1.6 mA	>3 kΩ	0.2 μs to 0.01%
	4053			0 to −10 V; +5 to −5 V [11]	>0.3 Ω	1 μs to 0.01%
	4054	12-bits	BIN; OBIN	0 to +3.2 mA; −1.6 to +1.6 mA	>3 kΩ	0.4 μs to 0.01%
	4055			0 to −10 V; +5 to −5 V [11]	>0.3 Ω	1 μs to 0.01%

	Model	Resolution	Input Code (T^2L/DTL Compatible)	Output	Output Impedance	Noise (RMS)	Glitches (peak) max.	Overshoot max.	Settling Time/ 10 V Step	Slew Rate
	4002	14-bits (incl. sign)	Mag & Sign BIN	±10 V	0.1 Ω	0.1 mV	±5 mV	±5 mV peak	20 μSec [8]	1.8 V/μSec
Deglitched	4015	12-bits	OBIN; 2 SC	±10 V	0.1 Ω	0.5 mV	±20 mV	25% for ⩽1 V Step	5 μs [10] to 0.01%	8 V/μSec
	4017	13-bits								

	Model	Resolution	Input Code (T^2L/DTL Compatible)	Analog Reference Input	Input Impedance min.	F.S. Output max.	F.S. Gain	Output Impedance	Settling Time Digital	Settling Time Analog
Multiplying	4028	8-bits	BIN	±10 V	3 kΩ	±10 V	(−255/256)	⩽1 Ω	5 μSec	5 μSec
	4029	10-bits					(-1023/1024)			

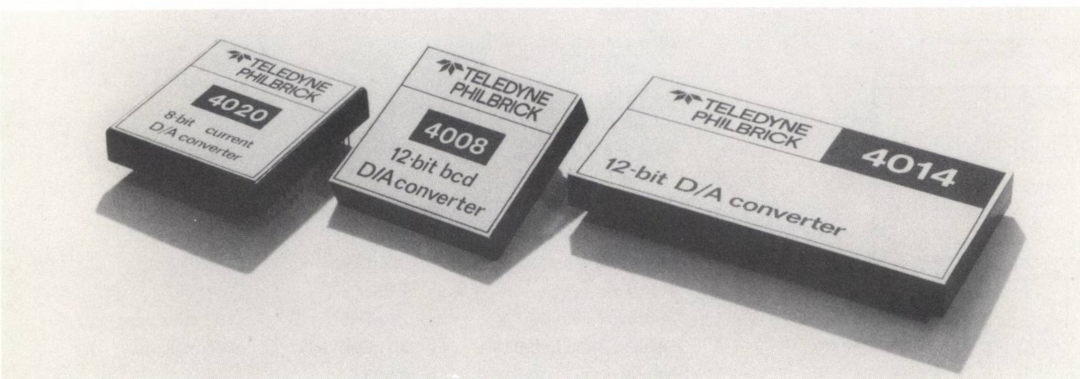
All specifications are typical at 25 °C nominal power supply unless otherwise indicated.

1. ABBREVIATIONS
   BIN – Binary
   OBIN – Offset Binary
   BCD – Binary Coded Decimal
   2SC – Two's Complement
2. Differential Linearity
3. Full Scale T.C. using internal feedback resistor.
4. 1 TTL Load equals −1.6 mA max. at V_{IN} = +0.4 V (Lo) and 40 μA max. at 2.4 (Hi).
5. All control inputs, outputs, and data output lines are compatible with standard DTL/TTL levels. Logic state switch '0' is <+0.8 V; logic state switch '1' is >+2.0 V.
6. Operating temperature range for all models, except model 4002 and the MIL-Grade Microcircuits, is 0 °C to +70 °C with a storage temperature range of −55 °C to +100 °C. Operating temperature range for model 4002 is +15 °C to +45 °C.
7. Operating temperature range for the MIL-Grade Microcircuits is −55 °C to +125 °C with a storage temperature range of −65 °C to +155 °C. Industrial temperature versions are available. Consult factory for details.
8. To 1 LSB of final value, maximum. For a 1 LSB step settling time is 2 μSec.
9. Mating connector supplied: Cinch 250-22-30-170
10. Settling time for a 100 mV step is 200 nSec to ±2 mV of final value.
11. Also, +10 V to −10 V; +2.5 V to −2.5 V available.

Zero Offset, max. (Unipolar/Bipolar)	Nonlinearity @ 25 °C max.	Gain TC ppm/ °C max.	Stability Zero TC ppm/ °C max.	PSRR %/%ΔV_S max.	Power Requirements	Mechanical (Package & Socket) See pages 64-65
<50 nA/±½ LSB	±½ LSB	±40	±4	±0.05	±15 V @ 15 mA	E6 (6069)
±½ LSB			±20		±15 V @ 20 mA	
<50 nA/±½ LSB	±½ LSB	±40	±4	±0.05	±15 V @ 15 mA	E6 (6069)
±½ LSB			±20		±15 V @ 20 mA	
<50 nA/±½ LSB	±½ LSB	±30	±4	±0.05	±15 V @ 15 mA	E6 (6069)
±½ LSB			±20		±15 V @ 25 mA	
<50 nA	±½ LSB	±30	±4	±0.05	±15 V @ 15 mA	E6 (6069)
±½ LSB			±20		±15 V @ 25 mA	
<50 nA @ 70 °C	±½ LSB	±20	±3	±0.002	±15 V @ 15 mA	E6 (6069)
±½ LSB			±20		±15 V @ 25 mA	
<50 nA @ 70 °C	±½ LSB	±20	±3	±0.002	±15 V @ 20 mA	E6 (6069)
±½ LSB			±20		±15 V @ 25 mA	
<50 nA @ 70 °C	±½ LSB	±20	±3	±0.002	±15 V @ 20 mA	E6 (6069)
±½ LSB			±20		±15 V @ 25 mA	
4 μA	±½ LSB (2)	±20	±10	±0.002	±15 V @ 150 mA	E6 (6128)
±10 ppm of F.S.	±¼ LSB	±45 (3)	±10/±15	±0.002	±15 V @ 15 mA	S5 (6)
±20 mV/±30 mV			±25/±30		±15 V @ 20 mA	
±10 ppm of F.S.	±¼ LSB	±25 (3)	±10/±15	±0.002	±15 V @ 15 mA	S5 (6)
±20 mV/±30 mV			±15/±25		±15 V @ 20 mA	
±10 ppm of F.S.	±¼ LSB	±15 (3)	±10/±15	±0.002	±15 V @ 15 mA	S5 (6)
±20 mV/±30 mV			±10/±15		±15 V @ 20 mA	

Zero Offset, max.	Nonlinearity @ 25 °C max.	Gain TC ppm/ °C max.	Stability Zero TC ppm/ °C max.	PSRR %/%ΔV_S max.	Power Requirements	Mechanical (Package & Socket) See pages 64-65
Adj. to 0 V	±½ LSB	±7	±3	±0.007	±15 V @ 35 mA	E8 (9)
Adj. to 0 V	±½ LSB	±20	±10	±0.005	±15 V @ 150 mA +5 V @ 250 mA	E8 (9)

Zero Offset, max.	Nonlinearity @ 25 °C max.	Gain TC ppm/ °C max.	Stability Zero TC ppm/ °C max.	PSRR %/%ΔV_S max.	Power Requirements	Mechanical (Package & Socket) See pages 64-65
±2.5 mV	±½ LSB	±25	±10	±0.002	±15 V @ 25 mA	E6 (6069)



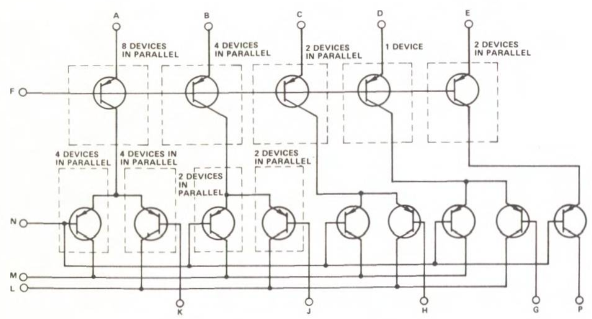
Monolithic Quad Current Switch

FEATURES

- 16 Bit Accuracy
- 0.5 ppm/°C Nonlinearity T.C.
- 30 nSec Settling to Within 0.01%
- High Current Capability
- 3 nSec Switching Speed
- Operates over +5 to ±15 V
- Low I_{CBO} of 6 pA

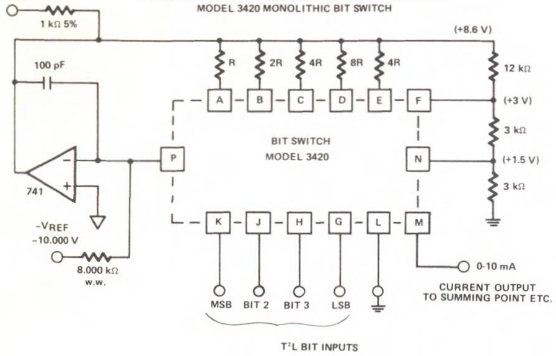
APPLICATIONS

- D/A and A/D Converters
- Meter Drive
- x - y Recorders
- Programmable Voltage Sources
- Micropower D/A Converters
- +5 Volt D/A Converter



MODEL 3420 SCHEMATIC DIAGRAM

TYPICAL APPLICATION CIRCUIT FOR TELEDYNE PHILBRICK MODEL 3420 MONOLITHIC BIT SWITCH



REVERSE PINS L & M TO GET COMPLEMENTARY OUTPUTS. HIGH = ON

Philbrick's new monolithic quad current switch Model 3420 is designed for data conversion applications where speed, accuracy, and stability are critical requirements. A switching speed of 3 nSec and a settling time of 30 nSec to 0.01% permit the design of high speed converters with up to 16 bit accuracy.

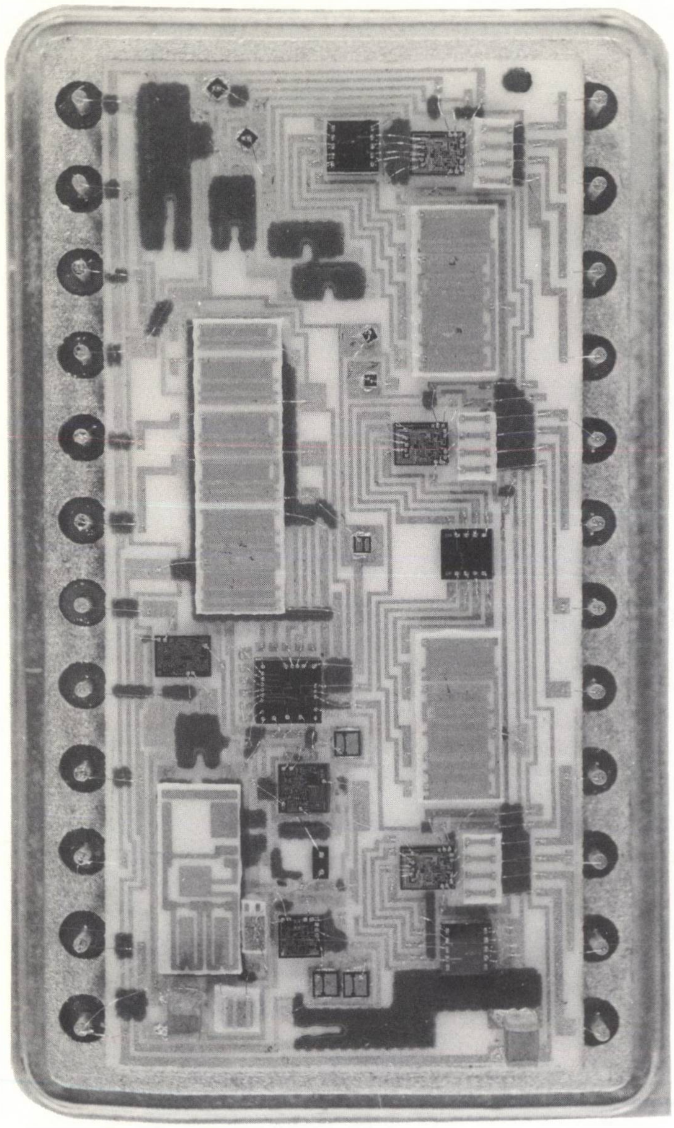
A combination of special topographical design and high quality PNP transistors is unique to the Philbrick 3420. This design technique* eliminates "thermal tails" and permits full scale output currents as high as 40 mA or as low as 40 μA. Precision matching of the PNP transistors and a superior reference capability ensures exceptionally low T.C. of nonlinearity.

Model 3420 quad switch can be processed to MIL-STD-883 for military or rugged commercial applications and is offered in a 14 pin dual-in-line package.

*Registered U.S. Patent Office

	TYPICAL	GUARANTEED
LOGIC INPUTS (T^2L)		
"0" (Switch Off)	––	0.8 V max, −40 μA
"1" (Switch On)	––	2.0 V min, +0.01 μA
OUTPUT CURRENT (For 4.0 mA F.S.)		
MSB (Bit One)	––	2.0 mA
BIT 2	––	1.0 mA
BIT 3	––	0.5 mA
BIT 4	––	0.25 mA
OUTPUT CURRENT RANGE		
Full Scale	1 μA to 40 mA	40 μA to 4.0 mA min.
Per Emitter	0.06 μA to 2.5 mA	2.5 μA to 0.25 mA min.
OUTPUT VOLTAGE		
For Rated Accuracy	−0.5 to −5 Vdc	0 to −3.0 Vdc min.
Derated	+10 to −20 Vdc	+0.5 to −10 Vdc min.
SWITCH CHARACTERISTICS		
β	230	100 min.
β Match	±1%	––
V_{BE} Match	±0.3 mV	––
$\frac{dV_{BE}\text{ Match}}{d\theta}$	––	2 μV/°C
$\frac{d\alpha\text{ Match}}{d\theta}$	2 ppm/°C	10 ppm/°C max.
I_{ebo} @ 3 V	4 pA	100 pA max.
I_{cbo} @ 5 V	6 pA	100 pA max.
DYNAMIC CHARACTERISTICS		
f_α @ 0.5 mA	160 MHz	––
Switching Time Uncertainty	0.2 nSec	––
Rise Time	2 nSec	––
Settling Time to 0.1%	21 nSec	100 nSec max.
Settling Time to 0.01%	30 nSec	300 nSec max.
Nonlinearity	0.008%	––
Nonlinearity T.C.	0.5 ppm/°C	2 ppm/°C
Trim Range	––	2000 ppm max.

Microcircuit Digital/Analog Converters



FEATURES

- 8/10/12-bit Resolution
- 0.8 ppm/°C Nonlinearity T.C.
- −55 to +125°C Temperature Range
- 2 μSec Settling time to ½ LSB of 12-bits (4055)
- Voltage or Current Output
- Hermetically Sealed
- Complete and Self-Contained
- Feature Philbrick's Proprietary Quad Switch

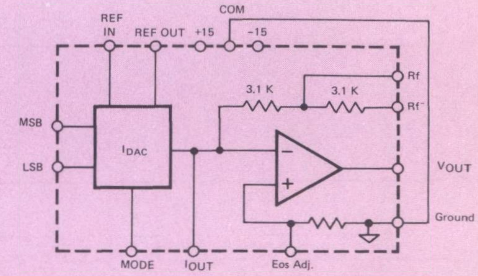
Philbrick's **4050** Series of microcircuit D/A Converters is designed for applications demanding high performance over a wide temperature range. Complete and self-contained, they include within a small 24-pin double-dual-in-line package (1.39"L × 0.80"W × 0.20"H), a precision reference, resistor network, current switches, and temperature compensation. Voltage output versions also include a high-speed output amplifier.

Models **4050**, **4052**, and **4054** are current output devices with 8, 10, and 12-bits resolution, respectively, which feature exceptionally fast settling time (0.4 μSec to within ½ LSB for 12-bits) and very low offset and full scale drift with temperature. The current output versions have built-in feedback resistors for use with external amplifiers.

Models **4051**, **4053**, and **4055** are the corresponding voltage output versions with 8, 10, and 12-bit resolution, respectively. Incorporated in the design of these DAC's is a special feedback network around the internal operational amplifier which permits the selection of two output voltage ranges in unipolar, and three voltage ranges in bipolar operation. The high speed output amplifier gives a settling time of 2 μSec to within ½ LSB for a full scale change.

All **4050** Series DAC's can be operated in the unipolar or bipolar mode. All models incorporate a special reference network and temperature compensation to ensure exceptionally low thermal errors. Hermetic sealing and the exclusive use of high quality components give the **4050** Series excellent reliability in the most demanding applications.

Military versions are also available processed to MIL-STD-883.

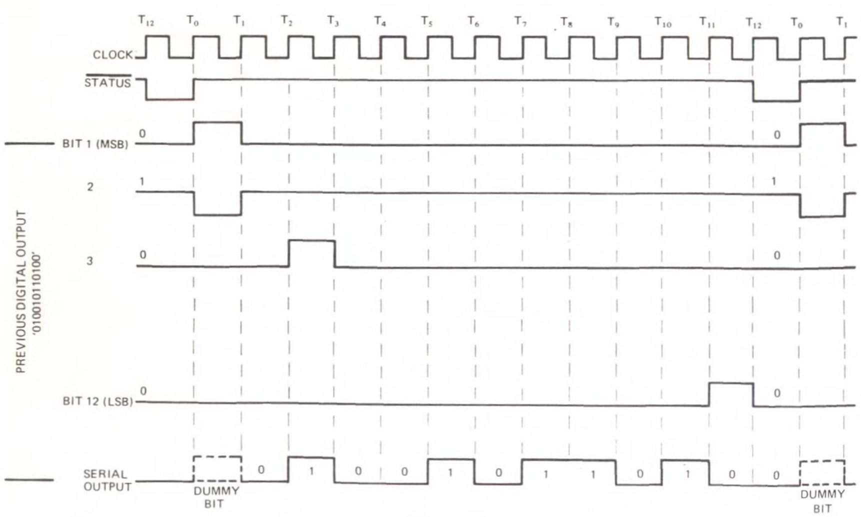


SERIES 4050 SCHEMATIC DIAGRAM

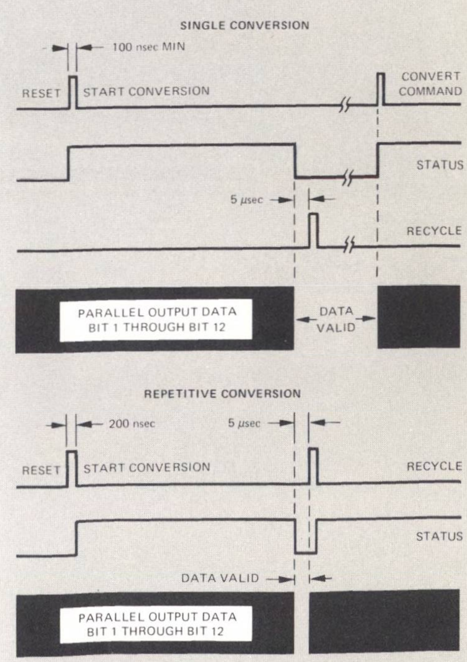
Analog/Digital Converters

		Model	Resolution	Linearity at 25°C max.	Analog Input Options	Output Code Options (T^2L/DTL Compatible)	Input Impedance	Conversion Time, max. (Throughput Time)
Tracking		4110	8-bits	±¼ LSB	0 to −10 V +5 to −5 V	BIN; OBIN	4 kΩ	125 ns/LSB
Successive Approximation	General Purpose Economy	4114	8-bits	±½ LSB	0 to −10 V +5 to −5 V	BIN; OBIN: 2S C	4.5 kΩ	45 μSec
		4113	10-bits				5 kΩ	30 μSec
		4112	12-bits				2 kΩ	60 μSec
	Low Cost High Performance	4105	8-bits	±½ LSB	0 to −10 V +5 to −5 V	BIN; OBIN: 2S C	2 kΩ	15 μSec
		4104	10-bits					20 μSec
		4103	12-bits					30 μSec
	High Speed	4108	8-bits	±½ LSB	0 to −10 V +5 to −5 V	BIN; OBIN: 2S C	2 kΩ	6 μSec
		4107	10-bits					7 μSec
		4106	12-bits					10 μSec
Integrating		4109	12-bits	±½ LSB	0 to −10 V	BIN	100 kΩ	6 mSec
		410910			0 to +10 V			
		4111	12-bits	±½ LSB	0 to −10 V	BCD	100 kΩ	2.5 mSec ⑤
		411110			0 to +10 V			

1. All specifications are typical at 25°C nominal power supply, unless otherwise indicated.
2. ABBREVIATIONS
   BIN – Binary
   OBIN – Offset Binary
   BCD – Binary Coded Decimal
   2SC – Two's Complement
   CF – Consult Factory
3. 1 TTL Load equals −1.6 mA max. at V_{IN} = +0.4 V (Lo) and 40 μA max. at 2.4 V (Hi).
4. All control inputs, outputs, and data output lines are compatible with standard DTL/TTL levels. Logic state switch '0' is <+0.8 V; logic state switch '1' is >+2.0 V.



Typical Timing Diagram of Repetitive Operation for Successive Approximation A/D Converters

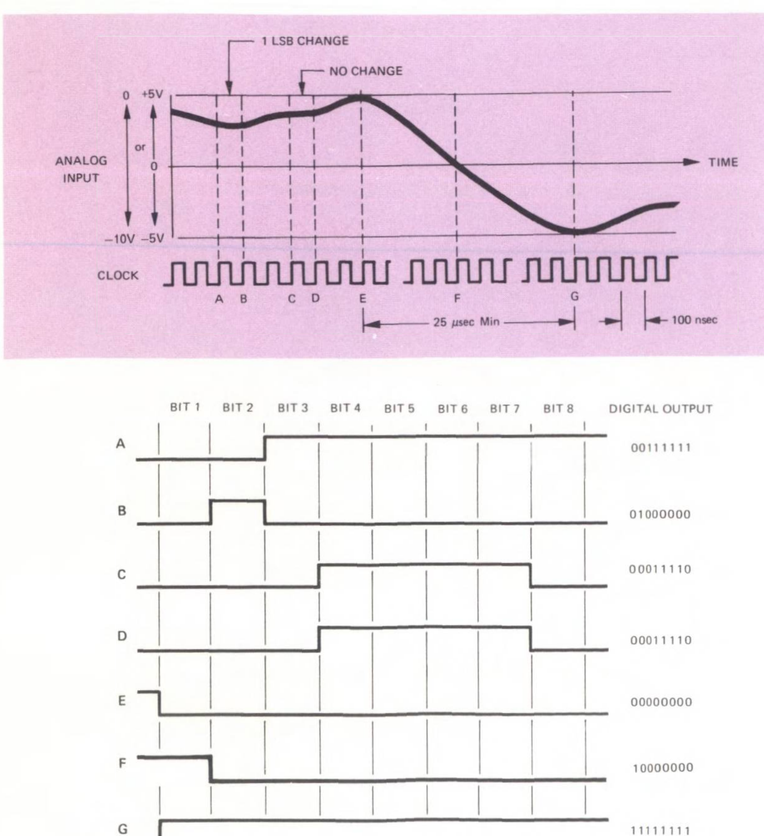


Timing Diagram for Integrating Models

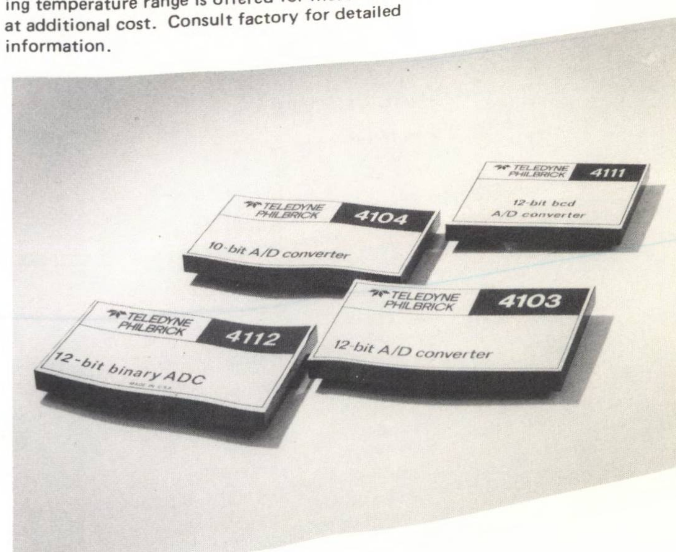
Zero Error max.	Gain Error max.	Gain TC ppm/°C max.	Stability Zero TC ppm/°C max.	PSRR %/%ΔV_S max.	Power Requirements	Mechanical (Package & Socket See pp. 64-65	
Trimmable to zero	+0%, −0.5%	±100	±2 ⑦	±0.05	±15 V @ 30 mA +5 V @ 150 mA	E7 (6122)	
±2 mV Unipolar ±5 mV Bipolar (Adj. to zero)	+0%, −1%	±40 ±40 ±30	±5 ⑦	±0.05	±15 V @ 50 mA +5 V @ 200 mA	E9 (6121)	
±2 mV Unipolar ±5 mV Bipolar (Adj. to zero)	+0%, −1%	±20	±5 ⑦	±0.001	±15 V @ 50 mA +5 V @ 200 mA	E9 (6121)	
±2 mV Unipolar ±5 mV Bipolar (Adj. to zero)	+0%, −1%	±20	±5 ⑦	±0.001	±15 V @ 50 mA +5 V @ 200 mA	E9 (6121)	
±5 mV (Adj. to zero)	+0%, −1%	±20	±3	±0.005	±15 V @ 30 mA +5 V @ 150 mA	E7 (6122)	
±5 mV (Adj. to zero)	+0%, −1%	±20	±3	±0.005	±15 V @ 30 mA +5 V @ 150 mA	E7 (6122)	

5. Includes a 100% overrange capability.
6. Scale Factor externally adjustable with 100 Ω rheostat (1 kΩ rheostat for models 4109, 410910, 4111, 411110) connected in series with E_{in} terminal.
7. Unipolar operation.
8. Operating temperature range for all models, is 0°C to +70°C with a storage temperature range from −55°C to +100°C.

For military type applications, an extended operating temperature range is offered for most models at additional cost. Consult factory for detailed information.



Timing Diagram for Tracking Model 4110



Voltage/Frequency Converters

FEATURES

- Resolution equivalent to more than 13 bits
- Linearity: ±0.008% (4701)
  ±0.015% (4703)
  ±0.0002% of F.S.
  Plus 0.02% of Signal (4705)
- Stability: ±27 ppm/°C (4701)
  ±44 ppm/°C (4703)
  ±47 ppm/°C (4705)
- High noise rejection
- DTL/T²L output; 10-load fan-out

APPLICATIONS

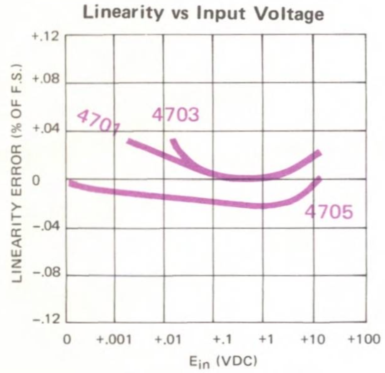
- Remote control or monitoring
- 2-wire digital transmission
- Electronic testing
- Magnetic tape recording
- Telemetering
- Isolation
- Servo loops
- Arithmetic operations
- Synchronous speed control

The Models 4701, 4703, and 4705 Voltage-to-Frequency Converters provide low-cost linear conversion of analog data to a digital pulse train whose repetition rate is proportional to the analog voltage.

The Models 4701, 4703, and 4705 feature advanced monolithic techniques in a modern adaptation of the "Precision Charge Dispenser" circuit principle. The result . . . uncompromised reliability and performance in a tiny, rugged plug-in module. Inherent noise rejection, plus output compatibility with standard or "COSMOS" DTL/²L logic, permits simple and dependable 2-wire digital transmission even through noisy environments to remote areas. Low OEM prices permit economical multiple signals using Models 4701, 4703, or 4705 at each sensor.

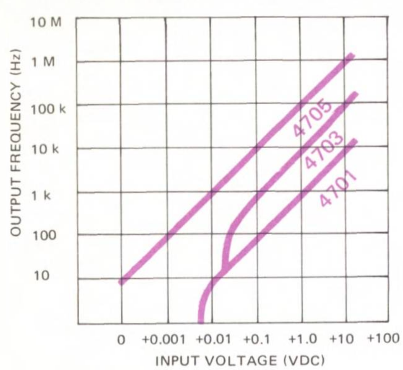
TYPICAL CURVES

Linearity vs Input Voltage

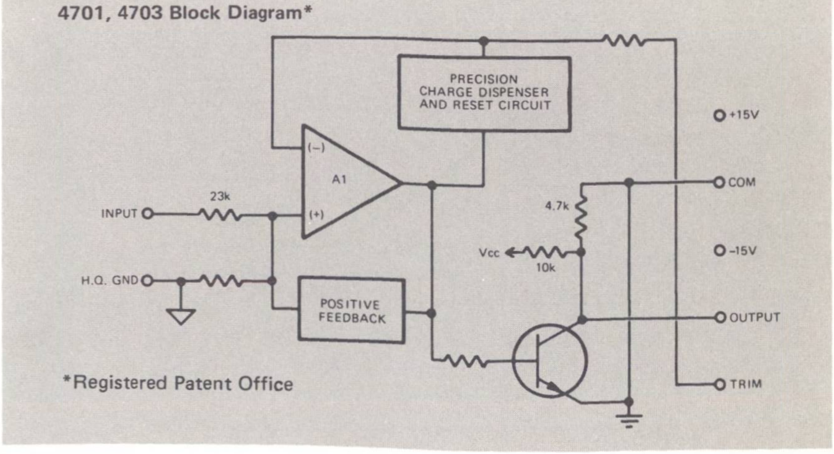


NOTE: Shaded area indicates Maximum error band

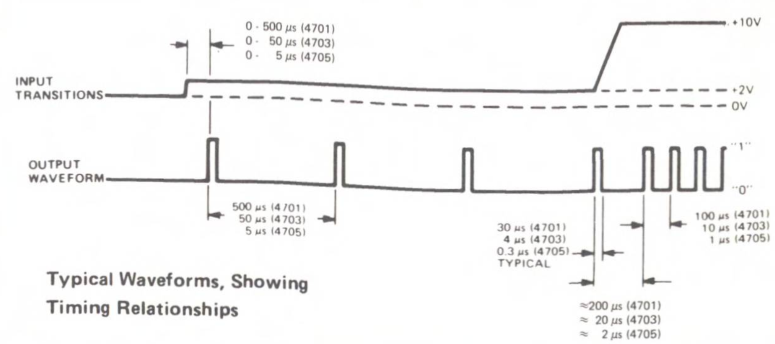
Voltage-to-Frequency Transfer Characteristic



4701, 4703 Block Diagram*



*Registered Patent Office

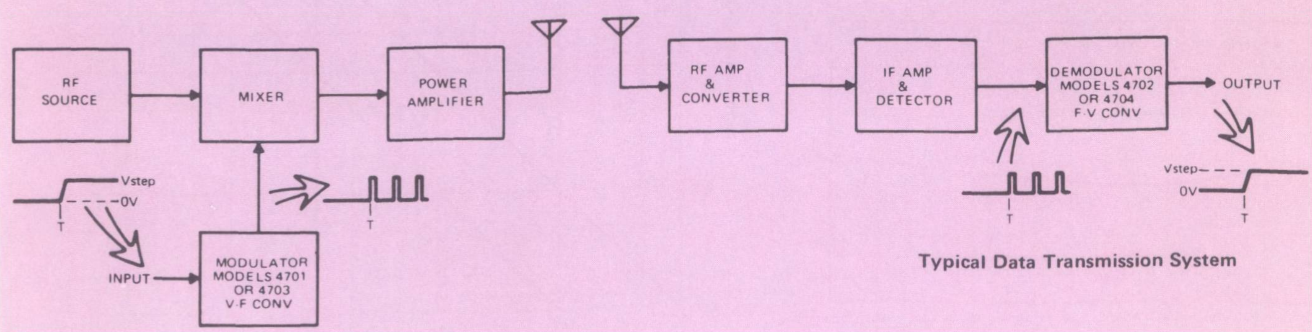


Typical Waveforms, Showing Timing Relationships

	4701	4703	4705
ANALOG INPUT			
Full Scale	0 VDC to +10 VDC ①		0 VDC to +10 VDC
Overrange	+10% min.		+5% min.
Configuration	Single-ended, referred to ground		Differential, referred to Ref IN
Offset Voltage (Adj. to Zero)	±3 mV typical; ±10 mV max.		±3 mV typical; ±10 mV max.
Impedance	23 KΩ nominal		10 kΩ nominal
Overvoltage Protection	±15 V max. input without damage		±150 max. input without damage
FREQUENCY OUTPUT			
Full Scale Frequency (f_{out})	10 Hz to 10 kHz, plus 10% overrange	100 Hz to 100 kHz, plus 10% overrange	1 Hz to 1 MHz, plus 5% overrange
Linearity	±0.008% typical; ±0.05 max.	±0.015% typical; ±0.05% max.	±0.001% typical; ±0.05% max.
Transfer Characteristic	f_{out} = 10 kHz x (Ein/10 V)	f_{out} = 100 kHz x (Ein/10 V)	f_{out} = 1 MHz x (Ein/10 V)
Full Scale Factor	9.900 V ±0.05 V (trimmable to 10.000 V for 10.000 kHz)	9.900 V ±0.05 V (trimmable to 10.000 V for 100.00 kHz)	9.900 V ±0.05 V (trimmable to 10.000 V for 1 MHz)
Waveform	Train of DTL/T^2L – compatible	Train of DTL/T^2L – compatible	Train of DTL/T^2L – compatible
Output Levels	Pulses, 30 μSec wide	Pulses, 3 μSec wide	Pulses, 0.3 μSec wide
"1" (HIGH)	+5 V ±0.5 V (no load); +2.4 V min. (+0.4 mA load)	+5 V ±0.5 V (no load); +2.4 V min (+0.4 mA load)	+5 V ±0.5 V (no load); +2.4 V min. (+0.4 mA load)
"0" (LOW)	+0.10 ±0.10 V @ –16 mA sink current	+0.10 ±0.10 V @ –16 mA sink current	+0.20 ±0.20 V @ –16 mA sink current
Output Impedance (In High)	3 kΩ	1 kΩ	680 Ω
Fan-out	10 standard T^2 L loads	10 standard T^2 L loads	10 standard T^2L loads
Short Circuit Protection	Indefinitely to ground without damage	Indefinitely to ground without damage	Indefinitely to ground
RESPONSE			
Settling Time to 0.01%	1 to 2 cycles plus 20 μSec	1 to 2 cycles plus 2 μSec	1 to 2 cycles plus 10 μSec
Overload Recovery	10 msec	10 msec	1 msec
Allowable Capacitive Load	1000 pF for rated performance	500 pF for rated performance	100 pF for rated performance
STABILITY			
Full Scale (Span)			
T.C. (PPM/°C of F.S.)	±24 typical; ±100 max.	±44 typical; ±150 max.	±47 typical; ±200 max.
Drift			
Per Day	±100 PPM of F.S.	±100 PPM of F.S. max.	±100 PPM of F.S.
Per Month	±200 PPM of F.S.	±200 PPM of F.S. max.	±200 PPM of F.S.
Power Supply Sensitivity	±500 PPM/1% Δ V_{CC} max.	±500 PPM/1% Δ V_{CC} max.	±500 PPM/%ΔV_{CC} max.
Input Offset			
T.C. (PPM/°C of F.S.)	±3 typical; ±10 max.	±3 typical; ±10 max.	±3 typical. ±5 max.
Drift			
Per Day	±10 PPM of F.S.	±10 PPM of F.S.	±10 PPM of F.S.
Per Month	±20 PPM of F.S.	±20 PPM of F.S.	±20 PPM of F.S.
Power Supply Sensitivity	±100 μV/% Δ V_{CC} max.	±100 μV/% Δ V_{CC} max.	±100 μV/%ΔV_{CC} max.
Warm-up Time	<1 minute to 0.01%	<1 minute to 0.02%	<5 minute to 0.02%
POWER	±15 V @ ±12 mA	±15 V @ ±18 mA	±15 V @ ±32 mA
ENVIRONMENTAL			
Temperature			
Rated		0 °C to +70 °C	
Derated		–40 °C to +85 °C	
Storage		–55 °C to +125 °C	

① Input voltage of Model 470110 is 0 V to –10 V. Other specifications identical to 4701. Price $64.00 (1-9).

Specifications are typical at +25 °C, V_{CC} @ ±15 V, unless otherwise indicated.



Typical Data Transmission System

Frequency/Voltage Converters

FEATURES

- Excellent Linearity 0.008%, Typ. (4702)
  0.006%, Typ. (4704)
- Low Cost
- Accepts DTL, TTL, HNIL, COSMOS, Sine, Square or Triangular Wave Inputs
- Adjustable Hysteresis for use with Small Signals
- 20 mA Output Rating

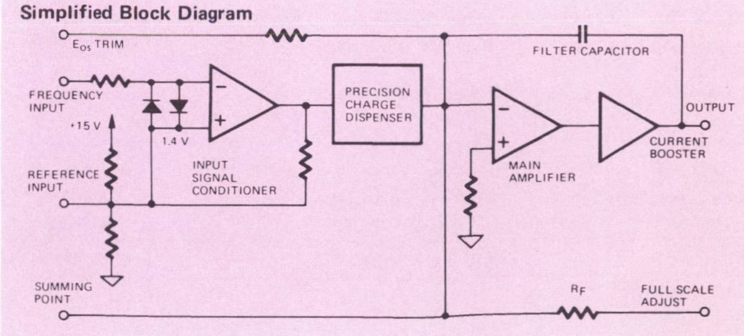
APPLICATIONS

- Magnetic and Optical Pickups
- Phase Locked Loops
- Telemetry Systems
- Frequency Monitors
- Remote Data Transmission
- Tachometers
- Flow Meters
- Broadband FM Discriminators
- Doppler Sonar & Radar
- Frequency vs. Amplitude X-Y Plot

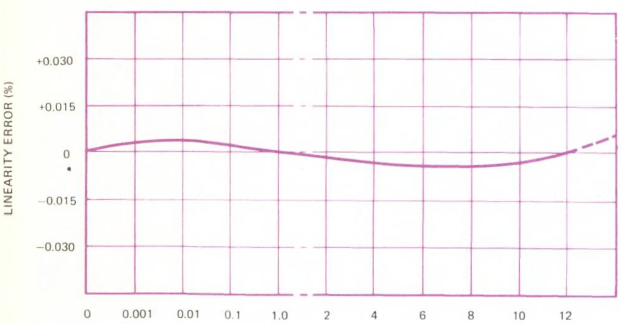
Models 4702 and 4704 Frequency-to-Voltage Converters provide low-cost linear conversion of frequency-coded information to a voltage whose amplitude is proportional to the frequency of the input signal. For maximum versatility the input is compatible with DTL, TTL, COSMOS, and High Noise Immunity Logic. Also, a minimum of external components can be used to adjust the hysteresis and biasing so that low level signals and sine-wave inputs can be accurately converted. If a scale factor change is required, an external resistor can be added to give a full scale output with input signals as low as 1 kHz with only a minor reduction in accuracy.

Models 4702 and 4704 can be used Philbrick Models 4701, 4703, and 4705 Voltage-to-Frequency Converters, to provide exceptionally accurate encoding and decoding of data.

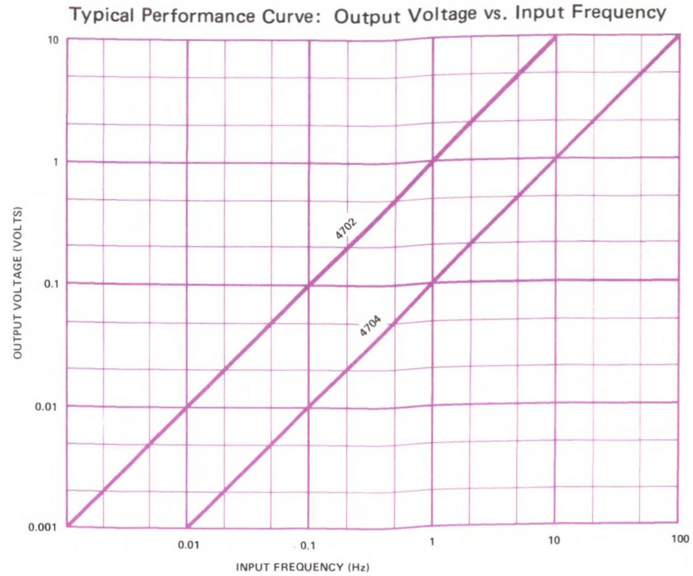
Simplified Block Diagram



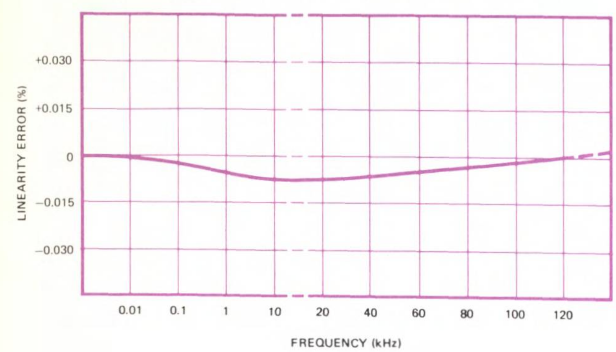
Model 4702: Nonlinearity vs. Input Frequency (Typical)



Typical Performance Curve: Output Voltage vs. Input Frequency



Model 4704: Nonlinearity vs. Input Frequency (Typical)

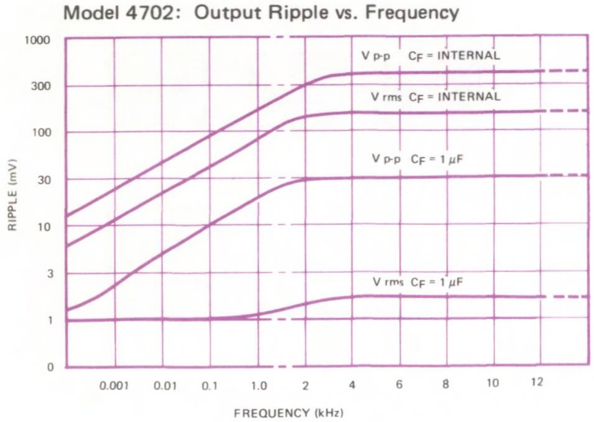


Typical at +25 °C, V_{CC} @ ±15 V, unless otherwise indicated.

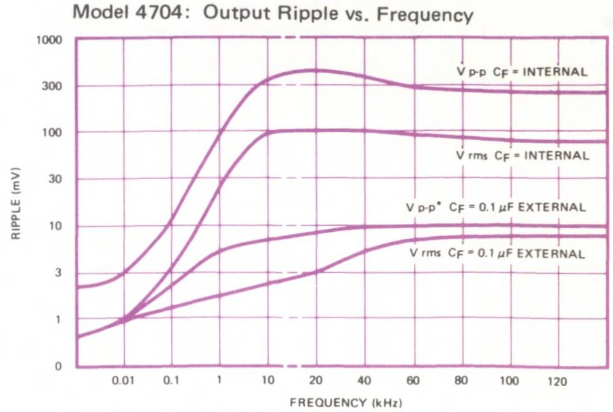
	4702	4704
FREQUENCY INPUT		
Full Scale	0 Hz to 10 kHz	0 Hz to 100 kHz
Overrange, min.	+10%	+10%
Input Levels ①	−12 V to +0.8 V = Low +2.0 V to +12 V = High (±15 V Fault ②)	−12 V to +0.8 V = Low +2.0 V to +12 V = High (±15 V Fault ②)
Loading	⩽1 TTL Load ②	⩽1 TTL Load ②
Input Pulse Width, min.	30 μSec for rated accuracy ③	2.5 μSec for rated accuracy ③
Input Impedance	15 MΩ ‖ 8 pF	3 kΩ ‖ 5 pF
ANALOG OUTPUT		
Full Scale Voltage	0 to +9.9 V ±0.1 V ④ (4702) 0 to −9.9 V ±0.1 V ④ (470210)	0 to +9.9 V, ±0.1 V ④
Offset, E_{OS}	±10 mV max. @ f = 0 Hz	±10 mV max. @ f = 0 Hz
Linearity	±0.008% Typ., ±0.03% max. f_{in} = 1 Hz to 11 kHz	±0.006% Typ;, ±0.05% max. f_{in} = 10 Hz to 110 kHz
Output Impedance, max.	0.05 Ω, <0.005 Ω Typ.	0.1 Ω, 0.01 Ω Typ.
Ripple	25 mV p-p @ f = 1.0 Hz 170 mV rms @ f = 10 kHz	50 mV p-p @ f = 10 Hz 70 mV rms @ f = 100 kHz
Output Current, min. ⑤	+20 mA @ V_O = +10 V, (4702) −20 mA @ V_O = −10 V, (470210)	−5 to +20 mA (V_O = 0 to +10 V)
RESPONSE		
Filter Time Constant,	0.24 mSec; can be increased with ext. cap.	0.02 mSec; can be increased with ext. cap.
STABILITY		
ΔE_{OS} vs. Temperature,	±50 μV/°C (±5 ppm/°C)	±50 μV/°C (±5 ppm/°C)
$\Delta E_{OS}/\Delta V_{CC}$, max.	±50 μV/% (±5 ppm/%)	±50 μV/% (±5 ppm/%)
ΔE_{OS}/Time	30 μV/day, 100 μV/month	30 μV/day, 100 μV/month
ΔV_{fs} vs. Temp., max.	100 ppm/°C	150 ppm/°C
$\Delta V_{fs}/\Delta V_{CC}$	300 ppm/%	300 ppm/%
ΔV_{fs}/Time	10 ppm/day, 30 ppm/month	10 ppm/day, 30 ppm/month
POWER		
Voltage (V_{CC})	±15 V, ±5% (±12 to ±18 V with derated specs)	±15 V, ±5% (±12 to ±18 V with derated specs)
Quiescent Current, max.	±12 mA (no load),	±22 mA (no load),
ENVIRONMENT & RELIABILITY		
Temperature	0 to +70 °C Rated −40 to +85 °C Derated −55 to +125 °C Storage	
MECHANICAL	E5	

1. Hysteresis: 400 mV p-p. nominal
2. Compatible with TTL and DTL Logic. Compatibility with High Noise Immunity Logic (HNIL) or COSMOS can be achieved with a noise immunity as large as 6 V by the addition of an external resistor.
3. Applies to both normally high dc levels with negative-going pulse trains, or to normally low dc levels with positive-going pulses. The rise and fall times are not critical.
4. At 500 Ω Rated Load. Trimmable to +10.000 V or −10.000 V (470210) with an external 500 Ω rheostat at rated input frequency.
5. Output short circuit proofing: indefinite to ground or to +15 V or to −15 V (470210); 5 seconds max. to −15 V or to +15 V (470210).
6. Input duty cycle recommended 25% to 75% for 100 kHz, 3% to 97% for 10 kHz.

Model 4702: Output Ripple vs. Frequency



Model 4704: Output Ripple vs. Frequency



*This Vp-p at CF = 0.1 μF does not include 80 mV peak spikes ~0.5 μsec wide, only the "ripple."

High Speed Sample Hold Amplifier

FEATURES

- ±1 nSec Max. Aperture Uncertainty Time
- 1 μSec Acquisition Time to 0.01%, Max.
- 0.005% Linearity
- 300 ns Settling Time to 0.01%
- 1 mV Maximum Feedthrough
- 20 kHz Bandwidth

APPLICATIONS

- Data Acquisition Systems
- A/D Converters
- D/A Converters
- Deglitch Circuits

DESCRIPTION

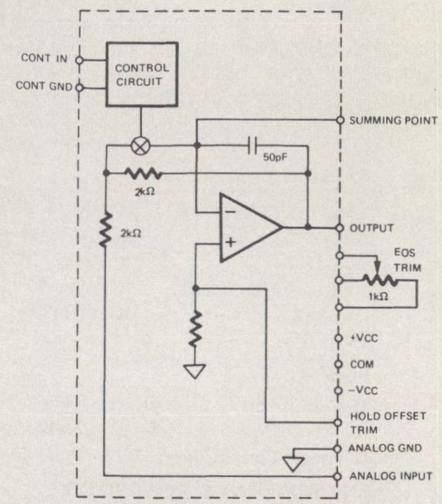
Model 4853 is a precision high-speed sample-hold amplifier especially designed for high-resolution data conversion systems. A guaranteed acquisition time of 1 μSec to 0.01% and other electrical characteristics of exceptional stability and accuracy recommend the 4853 for use with fast 12-bit D/A and A/D converters. Low feedthrough characteristics permit high throughput multiplexing regardless of input signal amplitude or frequency, thus achieving higher system speed without sacrificing resolution.

Model 4853 achieves high performance by innovative circuit design and exclusive use of high quality components. The switching circuit (a proprietary Philbrick design) minimizes aperture time and aperture time uncertainty. The low uncertainty time (±1 nsec, maximum) ensures a lower holding error for a given input $^{dv}/_{dt}$.

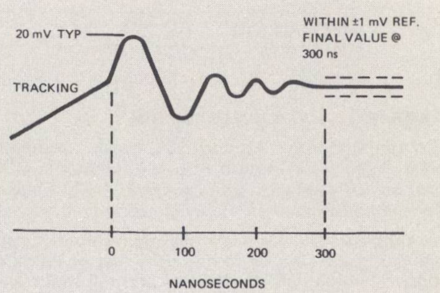
The gain of model 4853 is −1.000; i.e. the output is a precise inversion of the input.

For exceptionally demanding applications, the 4853 can be externally trimmed for zero offset and gain error. In circuits where speed is not essential (such as Analog-Digital converters with a long conversion time) the decay rate can be reduced by adding an external capacitor.

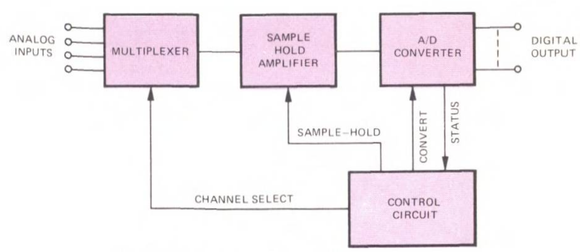
For optimum reliability the 4853 employs input and output short circuit protection. Internal shielding is incorporated to minimize the effects of electrostatic interference and epozy encapsulation rejects environmental effects for high reliability.



Simplified Block Diagram



Transients and Settling Time Switching to Hold



Typical Multiplexer with Sample-Hold Application

SPECIFICATIONS (Typical at +25°C, V_{CC} @ ±15 V, unless otherwise indicated)

INPUT	
Analog:	
Voltage	±10 V
Current	±5 mA
Impedance	2 kΩ ∥ (20 pF series 2 kΩ)
Digital:	
Sample	> +2.0 V (1 TTL load)
Hold	< +0.8 V (1 TTL load)
TRANSFER CHARACTERISTICS	
Nonlinearity, max	±0.005%
Gain (nominal at dc)	−1.000
Gain Error, max	±0.05% ①
Gain vs Temperature Range, max	10 ppm/°C
Sample Voltage Offset, max	3 mV ①
Sample Voltage Offset vs Temp. Range, max	150 µV/°C
Hold Voltage Offset, max	3 mV ① ⑤
Hold Voltage Offset vs Temp. Range, max	200 µV/°C
Hold Jump Voltage	±1 mV ①
Decay Rate, max	1 µV/µSec ②
Feedthrough (in Hold)	1 mV
PSRR (tracking), max	0.001%/% Δ V_S
(single - ended)	0.01%/% Δ V_S
Long Term Stability (per year)	0.01%
DYNAMIC CHARACTERISTICS	
Output	±10 V @ ±5 mA
Bandwidth (referred to dc gain), max	20 kHz to ±0.02% (80 kHz to −0.1% typ)
Slew Rate	30 V/µsec
Aperture Time (ref. to signal input), max	0 to 10 nsec
Aperture Uncertainty Time, max	±1 nsec
Acquisition Time	
(10 V step) to 0.01% F.S. max	1 µsec
(10 V step) to 0.1% F.S.	600 nsec
(20 V step) to 0.01% F.S. max	1.5 µsec
(20 V step) to 0.1% F.S.	1 µsec
Sample to Hold Transient	20 mV
Settling Time Switching to Hold	
to 0.01% F.S., max	300 nsec
to 0.1% F.S.	100 nsec
Phase Shift, max	0.01° at 20 kHz
POWER REQUIREMENTS	
Voltage	±15 V, ±2%
Current (quiescent) max	±30 mA
TEMPERATURE RANGE	
Operating: Rated	0°C to +70°C
Storage	−55°C to +125°C

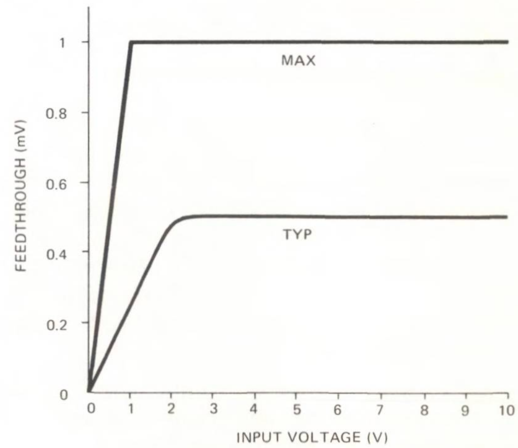
Notes:

① Trimmable to zero.
② May double each +10°C, ref. +25°C.
③ Full Scale is considered to be 10 V, therefore 0.01% is 1 mV.
④ Warm-up Time for Model 4853 is typically 10 minutes.
⑤ Worst case conditions for Sample Voltage Offset and Hold Jump Voltage will not occur simultaneously.

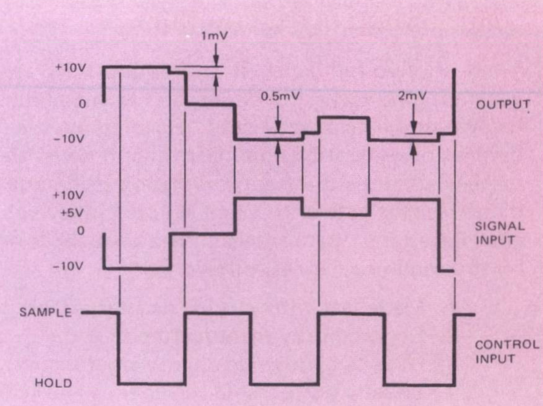
The Importance of Feedthrough

The typical data acquisition system consists of an input multiplexer followed by a sample-hold amplifier which buffers an analog-to-digital converter. If the sample-hold has a high feedthrough, a changing input signal will significantly affect the output. The multiplexer, therefore, cannot be switched during the ADC's conversion time without causing intolerable error, thus limiting data through-put.

The 4853's exceptional feedthrough characteristics are nonlinear and independent of frequency. A clamping network is used to limit the feedthrough to ±1 mV maximum for a 20 volt input step. This permits increased through-put in data acquisition systems.



Feedthrough Characteristics



Example of Feedthrough in Multiplexer Application

NONLINEAR PRODUCTS

Many natural processes are neither linear nor quantitative but behave in continuously smooth, nonlinear ways. To the systems engineer faced with solving nonlinear applications, Teledyne Philbrick offers a wide variety of circuit modules. Armed with a basic knowledge of operational amplifier theory, the engineer can easily understand and apply these nonlinear function modules to extend the mathematical versatility of op amps and provide exponential, transcendental, and high order functions.

Just as the gain is varied in a linear circuit by varying the ratio of the feedback impedance to the input impedance, so does the ratio of impedances for nonlinear circuits, but instead of being a fixed value its varitations, determined by the input amplitude: Also, nonlinear function circuits have basic limitations similar to those of operational amplifiers; dynamic range, bandwidth, conformity, voltage offset, etc.

WHAT IS A NONLINEAR CIRCUIT?

A circuit is nonlinear when the output is not linearly proportional to its input. Obviously, all digital circuits and amplifiers with unintentional distortion fall in this category; but these are not the products to be discussed here. Rather, we are interested only in those amplifiers having intentional, accurately predetermined, stable distortion. Usually for circuit modules the shape of the distortion can be accurately described by a simple and useful mathematical expression.

The products that we are mainly interested in are logarithmic devices, sine and cosine functions, square law modules, and multiplier/divider modules. Also available are modules whose output can be user-adjusted to virtually any function of the input. These are known as variable function modules.

VARIOUS CIRCUIT TECHNIQUES

There are two fundamental techniques which are used in generating nonlinear functions, and each technique has its own unique characteristics. Historically, the first method of generating nonlinear functions was the piece-wise, straightline approximation technique using diode-resistor networks which resulted in several advantages and disadvantages. The advantages offered by this technique are as follows:

1. Made fast with varying degrees of "accuracy."
2. Economically manufactured.
3. Used to synthesize almost any function.
4. Usually quite stable versus time and temperature.
5. Generally offers low noise.

The disadvantages include:

1. Narrow input dynamic range.
2. Inputs usually requiring full-scale inputs of at least 10 volts.
3. Output cannot be differentiated (passed through a high pass filter) since the first and greater derivatives are dicontinuous; glitches will appear in the differentiated output.

The second technique used in generating nonlinear functions is the continuous method which uses the nonlinear voltage/current characteristics of semiconductor materials and junctions such as used in log modules and transconductance multiplier/divider modules. The advantages offered by this second technique are as follows:

1. Wide input dynamic range.
2. Usually built compactly.
3. Cost can be very low.
4. Speed is moderate.
5. Output can be differentiated.

The disadvantages include:

1. Elaborate temperature compensation, internal or external, is required.
2. High output noise for certain functions.
3. Choice of desired functions is limited.

The first step in choosing a nonlinear module is to determine which of the two methods of nonlinear generation is most suitable for the application. Of course, some applications require modules with performance beyond the present state-of-the-art. If this is the case, reduced performance or another method should be considered.

WHAT IS ACCURACY?

Next to cost, the most important consideration for the customer engineer is some figure of merit, usually dubbed "accuracy," which he can use to calculate his overall system error. "Accuracy," however, is a rather nebulous term when applied to intentionally nonlinear operations. The term is primarily suited for defining error of straight-line phenomenon in terms of only **three** simple parameters: **offset, slope,** and **deviations** from straight-line. With linear circuits it is easy to select a reference to which errors can be compared in order to generate an accuracy specification. However, for nonlinear operations, it is necessary to look at the general case from which accuracy is derived, using some simple assumptions.

In the general case, error must be defined in terms of three more complex parameters: **offsets, curvature,** and **deviation** from ideal curvature, whereas the curvature is just a straight-line for the linear case. Also, in the general case, **no** assumptions can be made about the proportionality of input and output offsets which would allow the combination of error contributions by simple addition. To more easily understand the error definition, the input and output must be treated separately. It is really meaningless to combine the two errors for an overall accuracy specification because it depends on the amplitude of the input. As a result, it is necessary to calculate accuracy for the various regions or decades of input from the following general transfer function:

$$E_o = E_{o_{ref}} F \left[\frac{(I_{in} \pm I_{os})}{\pm I_{ref}} \right] - E_{oos}$$

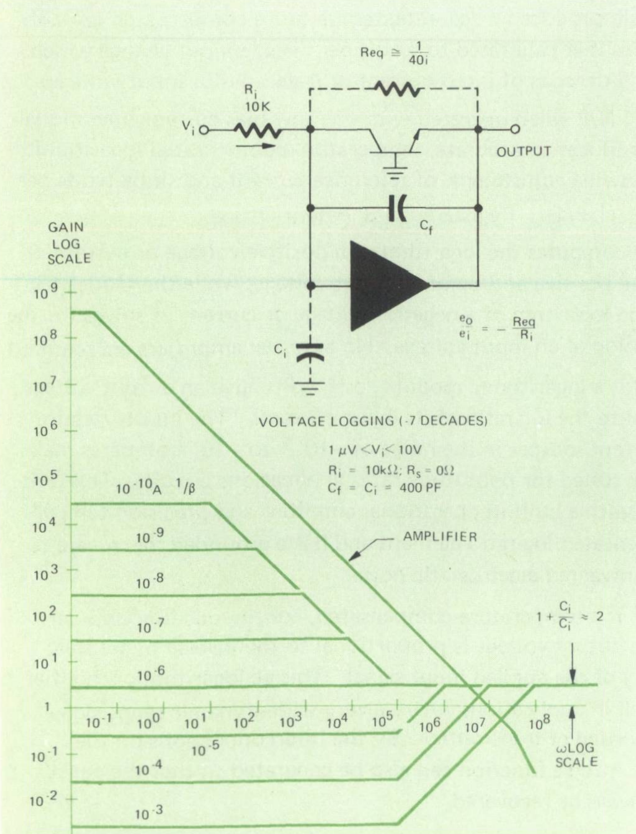
For functions with more than one input variable, such as log-ratio circuits, multipliers, and dividers, each of the inputs must be associated with its own, like-dimensioned (voltage/current), offset and reference.

The output and its tolerance can be easily calculated under any condition with the above relationship as a foundation, provided the magnitude, tolerance, temperature coefficient, and power supply dependence of both the input and output references and offsets are known. If the deviation from true function conformity is also considered, probable error and worst case errorbands can be calculated over the entire input range in any application. In other words, the most important specifications to the user is a unique combination of those specifications which take into account the user's particular requirements including **dynamic range, temperature range, power supply variations,** and any other relevant considerations.

LIMITATIONS WITH FREQUENCY

We have only been looking at the steady-state or low-frequency operation in determining optimum performance. For high frequency operations, additional considerations are necessary.

For linear systems, the simple parameters of small-signal gain-bandwidth product and output slewing rate are generally sufficient, since the gain is constant, and, therefore, bandwidth is constant. However, in nonlinear circuits, the small-signal gain (or slope) is a function of input level. Therefore, since the gain-bandwidth product tends to remain constant, the small-signal bandwidth will change as a function of input level. Example:



Small Signal Bandwidth vs. Input Level

For an amplifier with a 10 MHz gain-bandwidth product at a current level of 1 nA, the maximum operating frequency is approximately equal to 100 Hz.

Similarly, the slewing rate tends to be proportional to small-signal bandwidth. Therefore, slewing rate also changes as a function of input level. Generally, slewing time from one level to another level becomes proportional to the small-signal bandwidth at the final level. In other words, if it takes a certain amount of time in seconds to go from 1 nA to 10 nA then it will take approximately 10 times longer to go from 10 nA to 1 nA. One usually will find the small-signal bandwidths and slewing times are specified at several input levels.

PARAMETER DEFINITION AND MEASUREMENT GUIDE

SIX PARAMETERS are common to all nonlinear function elements and operators and their significance should be fully appreciated before any attempt is made to evaluate or predict their performance or the performance of a circuit using them.

- **Performance Range**
  States the values of input signal levels for which the specified input/output relationship will be maintained to the specified accuracy. Several ranges are possible, depending on accessories, the amplifier, and the circuit used.

- **Accuracy**
  Is stated in terms of conformance with the specified input/output function. It is frequently given in terms of the maximum per-unit or percent error, under "standard" conditions listed in the accuracy specification, and the error expression is usually a fairly simple function of the input (or output) signal level.

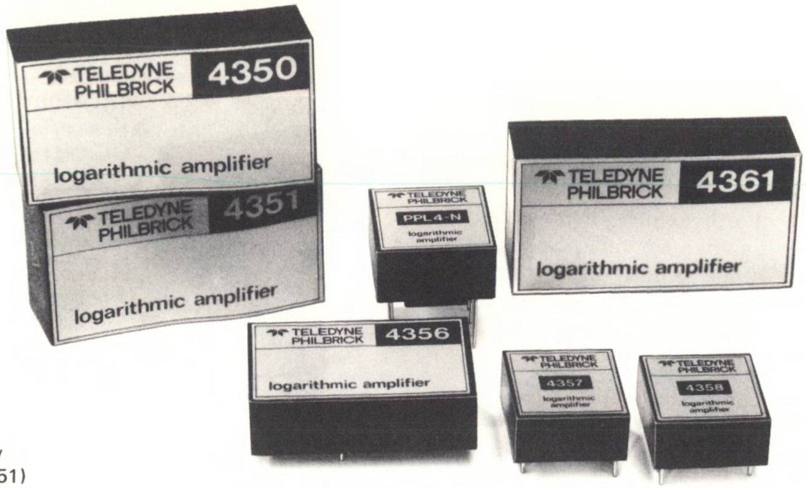
- **Temperature Coefficient**
  Relates the (steady-rate) ambient temperature to the worst-case error (at equilibrium, all other conditions being standard) in the input/output function.

- **Response Error**
  Relates the dynamic (small signal or transient) performance of the nonlinear element or operator to its dc (steady-state) performance; either by stating the (sinusoidal-wave) frequency rate over which the "standard conditions" performance will be maintained, or by stating a slewing rate, or a settling time.

- **Excitation Dependence**
  All nonlinear elements and operators require a near perfect signal source. When voltage is the independent variable, it should be supplied by the very low closed loop output impedance of an Operational Amplifier. When current is the independent variable, it should be provided by an Operational Amplifier programmed as a current pump.

- **Power Supply Dependence**
  Nonlinear elements and operators that require power supply potentials (such as synthesized function devices) should be used with accurate, well regulated supplies. To ensure optimum performance 0.05% absolute accuracy is recommended for the supply.

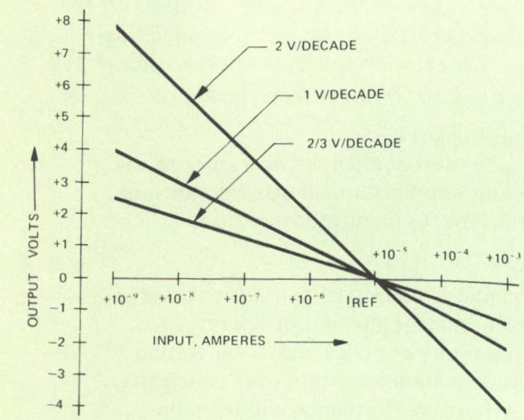
Logarithmic Amplifiers



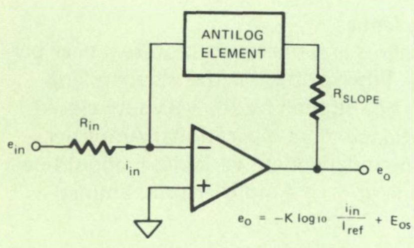
FEATURES

- Wide Dynamic Range
- Temperature Compensated
- Superior Logarithmic Conformity
- Very Low Cost (Models 4350/4351)
- Log or antilog obtained with built-in Operational Amplifier (Models 4350/4351)
- Adjustable Gain and Reference Current Controls (Models PPL4-N/P)
- Log of Current Ratio (Model 4361)
- Unique Nonlinear Module, $\sinh^{-1}$ Linear through Zero, then Three Decades of AC/DC Logging (Model 4356)
- 40 dB of Speech Compression (Model 4356)

BASIC CIRCUIT



LOG OF CURRENT (POSITIVE SIGNAL)



$$e_o = -K \log_{10} \frac{i_{in}}{I_{ref}} + E_{os}$$

WHERE K = SLOPE IN VOLTS/DECADE
i_{in} = INPUT CURRENT – e_{in}/R_{in}
I_{ref} = REFERENCE CURRENT
E_{os} = OUTPUT OFFSET VOLTAGE

Teledyne Philbrick logarithmic amplifiers provide an output proportional to the log or antilog of their input signal. (Model 4361 provides an output proportional to the log of its input signals only). Each unit is complete with a built-in operational amplifier and a precision antilog element, and requires only operating power plus input and output connections in order to perform its log or antilog computations.

Models 4357/4358 when utilized with two low-bias-current operational amplifiers will produce an accurate, temperature-compensated logarithmic ratio amplifier calibrated to 1 volt per decade input change which responds to 6 decades of input current or 4 decades of input voltage.

Models PPL4-N/P when operated with one low bias current operational amplifier, produces an accurate, temperature-compensated logarithmic amplifier allowing adjustment of reference current and slope (volts per decade input change). Registered U.S. Patent Office.

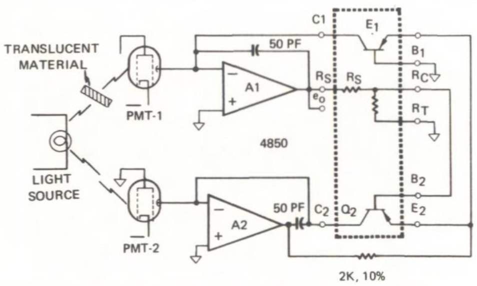
Model 4350 computes the logarithm of a positive voltage or current or solves for the positive antilog of an input voltage, while the Model 4351 computes the logarithm of a negative voltage or current or solves for the negative antilog of an input voltage. No external amplifiers are required.

Model 4361 is a logarithmic module designed to give an output voltage proportional to the log ratio of its input currents. The inputs require negative current sources in the range of -10^{-9} to -10^{-3} amperes making it ideally suited for phototube ratio applications circuits. This unit is complete with a built-in operational amplifier and precision temperature-compensated log-ratio element and has a grounded metal case to shield out unwanted electrostatic noise.

Model 4356 is a temperature-compensated, continuous-function network whose output voltage is proportional to the inverse hyperbolic sine ($\sinh^{-1}$) of the applied input signal. This ac logarithmic amplifier is very useful in applications where a very-wide-dynamic range signal must be recorded or transmitted. By the interconnections on the module, the inverse function can also be generated so that the exact information can be recovered.

	4357/4358	PPL4-N/P	4350/4351	4361
DYNAMIC RANGE				
Current	120 dB	120 dB	120 dB	120 dB
Voltage	80 dB	80 dB	80 dB	N/A
ACCURACY 1% OF READING (Referred to Input)				
1 nA to 10 nA	1%	2%	1%	0.5%
10 nA to 100 μA	1%	1%	0.5%	0.5%
100 μA to 1 mA	1%	2%	1%	1%
TEMPERATURE DRIFT				
Scale Factor				
+10 to +60°C	±0.04%/°C	–	–	–
–25 to +85°C	–	±0.04%/°C	±0.04%/°C	±0.04%/°C
Offset				
+10 to +60°C	±0.1 mV/°C	–	–	–
–25 to +85°C	–	±5 mV/°C	±0.3 mV/°C	±0.3 mV/°C
SLOPE				
Fixed	1 V/Decade	–	1,2,2/3 V/Dec	1 V/Dec
Adjustable	Yes	Yes	Yes	Yes
RATED OUTPUT				
Current	Depends on Amplifier	Depends on Amplifier	±10 mA	±5 mA
Voltage	Depends on Amplifier	Depends on Amplifier	±10 V	±10 V
BANDWIDTH				
1 nA	80 Hz	80 Hz	80 Hz	80 Hz
1.0 μA	Depends on Amplifier	Depends on Amplifier	70 kHz	70 kHz
10 μA	Depends on Amplifier	Depends on Amplifier	180 kHz	180 kHz
1 mA	Depends on Amplifier	Depends on Amplifier	200 kHz	200 kHz
CASE STYLE	A6	AS2	G2	G1
SOCKET	NSK–20	US–PP	NSK–20	NSK–9

1. Specifications are typical @ +25°C, nominal supply voltage, unless otherwise specified.



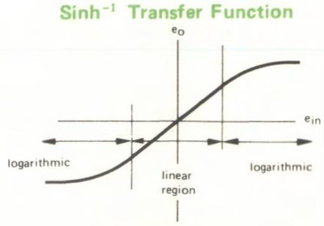
Translucent Measuring Circuit Application

An important application using the ratio of log ratio of two inputs is the measurement of the amount of light passing through translucent materials. It is interesting to note that although the intensity of the light source may vary due to temperature or age, the ratio output in decibels does not change because PMT-2 is used as a variable references. Since the material measured may vary from window glass to an opaque metal sheet, the advantage of a logarithmic output is easily recognized.

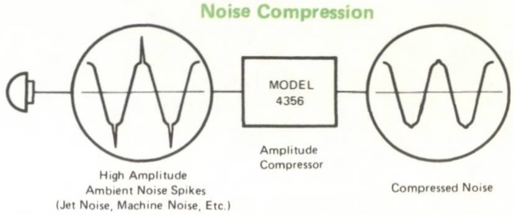
		4356
OUTPUT FUNCTIONS		
$Sinh^{-1}$	$Ksinh^{-1}\ \frac{I_{in}}{2I_r}$	I_{in} = 0 to ±5 mA; i_r = 1 μA ±2%
Log_{10}	$2.3\ Klog_{10}\ \frac{I_{in}}{I_r}$	I_{in} = 3 μA to ±5 mA; I_r = 1 μA ±2%
(K = 1.000)		Adj. with ext. Rf
CONFORMITY (100 Hz)		
$Sinh^{-1}$ (0.1 μA to ±5 mA)		0.5 dB
Log (±3 μA to ±5 mA)		0.5 dB
COMPRESSION		40 dB
INPUT		
Voltage		±10 V
Current		±5 mA
OUTPUT		
Voltage		±10 V
Current		±5 mA
BANDWIDTH		
Large Signal		10 kHz
TEMPERATURE STABILITY		
Offset		±2 mV/°C
Scale Factor		±0.01%/°C
Reference		±0.1 %/°C
TEMPERATURE RANGE		0°C to +70°C
POWER REQUIREMENT		
Voltage		±15 V
Current		±7 mA
CASE STYLE		E1
SOCKET		NSK-14

1. Specifications are typical @ +25°C, nominal supply voltage, unless otherwise specified.

$Sinh^{-1}$ Transfer Function



Noise Compression



This module is also useful in applications where a nonsaturating amplifier is needed such as in speech communication. Should the ambient noise be much greater than the desired input causing a linear preamplifier to saturate, the nonlinear amplifier will operate to keep the peak levels approximately constant.

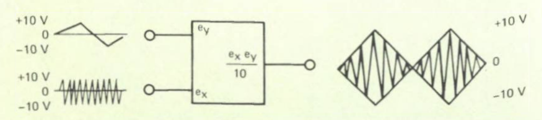
Multiplier/Dividers

FEATURES

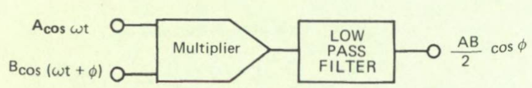
- 0.25% Accuracy
- 5 MHz Bandwidth
- 4 Quadrant Multiplication

APPLICATIONS

- Multiplying/Dividing
- Squaring/Square-rooting
- Root-mean-Squaring
- Suppressed Carrier Modulation
- Instantaneous Power Measurement

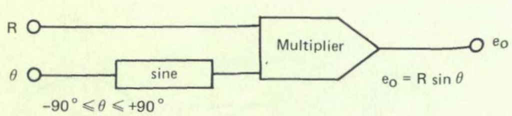


Amplitude modulator—suppressed carrier



Linear Phase Detector or Synchronous Detector

- Used in phase lock loop applications and phase angle measurements.



Altitude Circuit

- Applications of this circuit includes servo-mechanisms, telemetry, etc.

MODELS 4454, 4455, 4456, and 4457

Philbrick Models 4454, 4455, 4456, and 4457 variable transconductance multiplier/dividers achieve high performance without external amplifiers or trimming networks. Models 4454 and 4455 feature maximum full scale error (untrimmed) of 0.5% and 0.25% respectively. Models 4456 and 4457 are high speed units with 5 MHz bandwidth and a maximum untrimmed full scale error of 1% and 0.5% respectively. For all models the maximum error is specified for all four quadrants.

In combination with their high initial accuracy these multipliers exhibit exceptionally low drift due to temperature to keep a low total error budget. For the most demanding applications these units can be externally trimmed for feedthrough. In the division mode trimming is optional, but output offset voltage should be trimmed to ensure the widest dynamic range of operation.

The 4 quadrant analog multiplier is an extremely versatile device. The availability of low cost, high performance units has greatly increased the number and type of applications in all areas of industry. Philbrick's years of experience in applying analog technology have given our Applications Department the skills to solve the toughest applications problems. Therefor if you have any questions or need technical assistance, do not hesitate to contact us directly or through your local representative.

MODELS 4450 and 4452

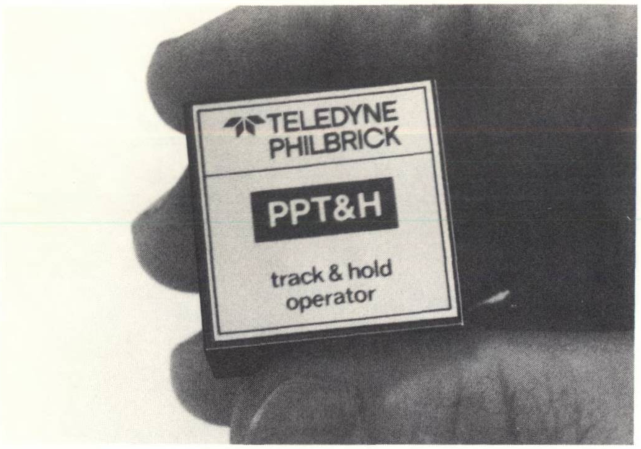
Model 4450 features a maximum error of 1% and a 1 MHz bandwidth. Model 4452, Philbrick's lowest cost multiplier features a maximum error of 2% in four quadrants, (1% in two quadrants) and a built-in division capability.

	HIGH ACCURACY		WIDEBAND		GENERAL PURPOSE ECONOMY	
	4454	4455	4456	4457	4450	4452
OUTPUT FUNCTION						
Multiply	XY/10	XY/10	XY/10	XY/10	XY/10	−XY/10
Divide	10 Z/X	10 Z/X	10 Z/X	10 Z/X	— —	−10 Z/Y
ACCURACY, % OF FULL SCALE TRIMMED						
4-Quadrant Operation, max.	+0.5%	0.25%	1%	0.5%	±1%	±2%
2-Quadrant Operation	— —	— —	— —	— —	— —	±1%
RATED INPUT						
Voltage—All Inputs	±10 V	±10 V	±10 V	±10 V	±10 V	±10 V
Impedance: X—Input	25 kΩ	25 kΩ	10 kΩ	10 kΩ	25 kΩ	40 kΩ
Y—Input	25 kΩ	25 kΩ	10 kΩ	10 kΩ	10 MΩ	30 kΩ
Z—Input	50 kΩ	50 kΩ	10 kΩ	10 kΩ	— —	90 kΩ
RATED OUTPUT						
Voltage	±10 V	±10 V	±10 V	±10 V	±10 V	±10 V
Current	±5 mA	±5 mA	±10 mA	±10 mA	±2 mA	±5 mA
BANDWIDTH						
−3 dB Response, min.	600 kHz	600 kHz	5 MHz	5 MHz	1 MHz	400 kHz
Full Output	50 kHz	50 kHz	1 MHz, min.	2 MHz, min.	100 kHz	50 kHz
1% Vector Error	5 kHz	5 kHz	300 kHz	100 kHz	— —	— —
TEMPERATURE STABILITY						
Output Offset, max.	0.5 mV/°C	0.2 mV/°C	1 mV/°C	0.5 mV/°C	±3 mV/°C	±3 mV/°C
TEMPERATURE RANGE	0 to +70°C	0 to +70°C	−25 to +85°C	−25 to +85°C	−25 to +85°C	0 to +70°C
POWER REQUIREMENTS						
Voltage	±15 V	±15 V	±15 V	±15 V	±15 V	±15 V
Current	±5 mA	±5 mA	±17 mA	±17 mA	±12 mA	±15 mA
CASE STYLE					A1	E5
SOCKET	6129	6129	6129	6129	NSK-20	NSK-20

Specifications are typical at +25 °C, nominal supply voltage, unless otherwise indicated

MODEL PPT&H

Track-and-Hold Operator



FEATURES

- High OFF Resistance – $10^{11}\ \Omega$
- Low ON Resistance – 300 Ω
- Fast Aperture Time – < 100 nsec
- Fast Acquisition Time – < 2 μsec

DESCRIPTION

The Model PPT & H Track and Hold Modulator is designed to function with all Teledyne Philbrick Operational Amplifiers and is optimized for use with FET input amplifiers. Performance, especially input current characteristics, will deviate from the specifications depending on the parameters of the amplifier selected. When used with a single operational amplifier, the overall circuit will track an input signal until a logic input is applied that opens the input, holding the output at the same level it had before switching.

SPECIFICATIONS

INPUT	
Voltage	±10 V
Impedance	ON–300 Ω OFF–$10^{11}\ \Omega$
SWITCHING DELAY GOING INTO HOLD	100 ns Typical
SWITCHING DELAY GOING OUT OF HOLD	<2 μsec
SWITCHING JUMP GOING INTO HOLD	$\frac{\pm 50 \text{ mV max}}{X}$ *
LOGIC INPUT	±1 V: +1V for track –1V for hold
POWER REQUIREMENT	
Voltage	±15V
Current	±1 mA
CASE STYLE	AS2
SOCKET	US-PP

$$* \quad X = \frac{C_{EXT} + 500 \text{ pF}}{500 \text{ pF}}$$

MODEL 4352

Avg-RMS-Vector Operator

FEATURES

- Calculating the square root of the sum of the squares of two signals
- Finding RMS values of a signal
- Finding average rectified values of a signal
- Plus, minus or AC input signal
- No external circuits required (trim control optional)

DESCRIPTION

The average–RMS–Vector Operator Model 4352 is a compact, encapsulated unit designed to: find the average value of an input signal, Y; find the RMS value of an input signal, X; or perform the operation $\sqrt{X^2 + Y^2}$ on the input signals X and Y. Averaging and RMS operation is based on instantaneous values of one input signal, with the output appearing as a positive voltage. The operation $\sqrt{X^2 + Y^2}$ is based on instantaneous values of two input signals. The output is a positive voltage, and is the instantaneous value of the function. Also by using two Model 4352 units, the operation $\sqrt{X^2 + Y^2 + Z^2}$ can be obtained. The small size and the multiple functions of which the Model 4352 is capable make it ideally suited for use as a computing element in the laboratory or in manufacturing equipment. Reliable accuracy is provided over a wide range of temperatures and operating conditions.

SPECIFICATIONS

OUTPUT FUNCTION	RMS	Average Rectified	$\sqrt{X^2 + Y^2}$
INPUT			
Voltage			
X	±10 V		±10 V
Y		±10V	±10 V
Current	0.75 mA	1 mA	
OUTPUT			
Voltage	±10V	±10V	±10V
Current	±2 mA	±2 mA	±2 mA
ACCURACY OF FULL SCALE	±3%	±1%	±1%
BANDWIDTH			
–3 dB	20 kHz	20 kHz	1 kHz
TEMPERATURE STABILITY		±0.1%/°C	
TEMPERATURE RANGE		0 to +75°C	
POWER REQUIREMENTS			
Voltage		±15 V	
Current		±30 mA	
CASE STYLE		G1	
SOCKET		NSK-9	

MODELS SPFX-N/P

Variable Function Elements

FEATURES

- ±0.1% Accuracy
- Temperature Compensated (<100 ppm/°C)
- Wide Bandwidth
- Output Function Adjustable by User

DESCRIPTION

The Models SPFX-N and SPFX-P are variable function elements consisting of ten-section temperature compensated, diode-resistor networks having uniformly spaced, fixed breakpoints. The desired function is approximated by eleven straight line segments whose slopes are adjusted by potentiometers accessible on the top of the case. The transition from one segment to the next occurs at one volt intervals of input voltage, from 0.5V to 9.5 V. When used in the recommended operational amplifier circuits, they will accept an input voltage and generate an output voltage proportional to the desired function. The function generated may be, to a good accuracy, any arbitrary continuous function.

Separate versions of the SPFX are available for positive going (SPFX-P) and negative going (SPFX-N) inputs. One of each may be used in combination for the generation of functions having inputs of both signs. When necessary, closer approximation may be achieved by incorporating additional SPFX units (having the same polarity gender) to obtain finer subdivisions of the curve.

SPECIFICATIONS

OUTPUT FUNCTION	User Adjustable	
Number of Segments	11	
Breakpoint Spacing	10 Breakpoints, ea 1V @ 0.5 V	
Accuracy when operated as square law device @25°C	$\lvert \delta_i / i_{max} \rvert < 0.001$, where δ_i = (i actual) – (i desired)	
INPUT		
Voltage	0 V to –/+10V	
Current	50 μA max	
OUTPUT		
Current	0 mA to –/+1 mA	
BANDWIDTH		
–3 dB Response	> 500 kHz	
TEMPERATURE STABILITY	<±100 ppm/°C	
TEMPERATURE RANGE	–25°C to +85°C	
POWER REQUIREMENTS		
Voltage	±15 V, ±0.01%	
Current	±3.5 mA	
CASE STYLE	SP	
SOCKET	MB-SP	Supplied

MODELS 4353/4354

Square Law Elements

FEATURES

- ±0.1% Accuracy
- Low Temperature Coefficient, <100 ppm/°C
- Wide Bandwidth

DESCRIPTION

The Models 4353 and 4354 are temperature compensated, straight-line approximation, ten-section diode function fitters that have break points adjusted to fit a square law relationship. They are designed to produce, to a good accuracy, an output voltage proportional to the square of the input voltage when connected to an appropriate operational amplifier. When used as the input network of an operational amplifier 4354 takes positive inputs and gives a negative output. When used as the feedback element of an operational amplifier to extract square roots, 4354 takes negative inputs and results in a positive output, while 4353 takes negative inputs and results in a negative output. Several applications using these modules include mean-square and RMS computation, odd-value or ab-squaring or rooting, and "quarter square" multiplication.

SPECIFICATIONS

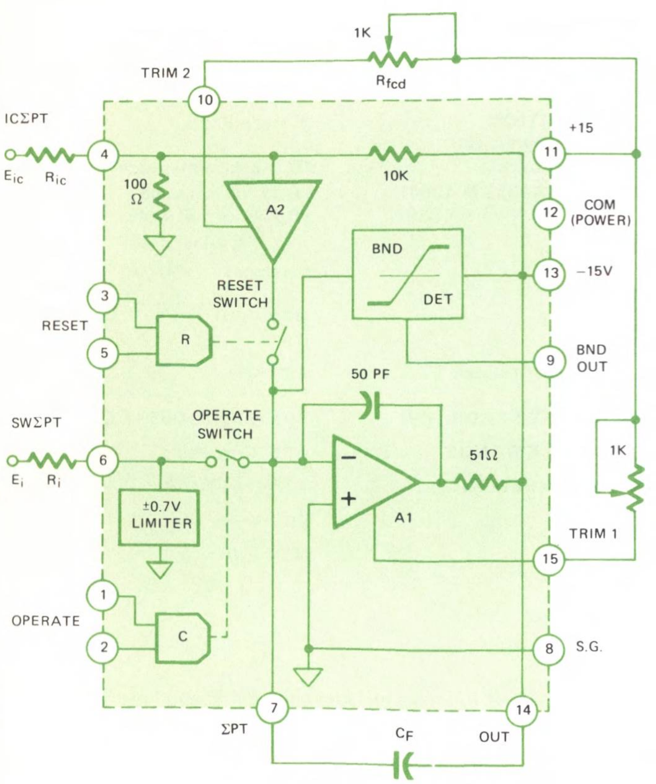
OUTPUT FUNCTION	$Y = +/-X^2$
Number of Segments	11
Breakpoint Spacing	10 Breakpoints, each 1 V @ 0.5 V
Accuracy ① (4353 & 4354)	±0.1% of full scale
(4359 & 4360)	±0.25% of full scale
INPUT Voltage	0 to –/+10 V
Current	Constant –/+50 μA
OUTPUT	0 to –/+0.5 mA
BANDWIDTH	
1% Absolute Accuracy ②	100 kHz
TEMPERATURE STABILITY	Typically ±0.005%/°C
TEMPERATURE RANGE	–25°C to +85°C
POWER REQUIREMENT	±15V, ±1.5 mA
CASE STYLE	E5
SOCKET	NSK–20

① Accuracy as a % of full scale includes gain, offset and linearity errors.
② Includes both phase shift and amplitude errors, measured at peak of 10V Triangle wave input

Three Mode Integrator

FEATURES

- Three Operating Modes, Reset/Integrate/Hold Track/Hold, Electronic Switch
- Command Signals can be of Positive or Negative Polarity
- Uncommitted Comparator Inputs Permit Compatibility to DTL/TTL Digital Logic and Gated Analog Logic
- Internal Bound Circuit Reduces Overdrive Recovery Time
- Accommodates Wide Range of Integrating Capacitors



MODEL 4850 BLOCK DIAGRAM

Model 4850 is a multi-purpose module which can be used as a three mode integrator, a track-and-hold circuit, or as an electronic SPDT switch. Mode control is accomplished by two uncommitted comparators, and external biasing can be introduced for compatibility with digital, analog, or special purpose logic. The comparator input command levels are compatible to many DTL, TTL levels; i.e., reference input may be elevated above common and interchanged respectively for inverse logic commands. The comparators control FET electronic switches that have excellent "feedthrough" characteristics, combined with typical RDS-ON resistances of 20 Ω for the Operate FET switch. The FET switches control the mode condition of the main FET amplifier, and the reset mode condition. A current amplifier drives the main amplifier. Both amplifiers and associated networks are in an internal reset (track) feedback loop. An internal bound circuit improves overdrive recovery with its output available. The operate mode gain configuration range is flexible with a wide integrating capacitor range of 0.001 μF to 10 μF. Input impedances in the order of 10^{11} Ω and ultra-low input bias currents in the FET amplifiers contribute to excellent three-mode integrating; low hold delay rates as a track (reset) and hold module. In the gated amplifier mode, the Model 4850 acts as an SPDT switch which can be commanded to select either one of two inputs and amplifier at arbitrary gains.

OPERATION–THREE-MODE INTEGRATOR

Model 4850 is principally designed to function as a three-mode integrator. Specifically, the module is capable of integrating a signal, holding the integral, and then resetting the output to zero or to some arbitrary initial condition. Operation in the integrate, hold, or reset mode is controlled by the polarity of the Operate FET switch (pin 1) or Reset FET switch (pin 3). During integration, the output of Model 4850 is represented by the following expressions:

$$E_0 = -\frac{1}{R_i C_f}\int_0^f E_i dt + KE_{ic}$$

where.

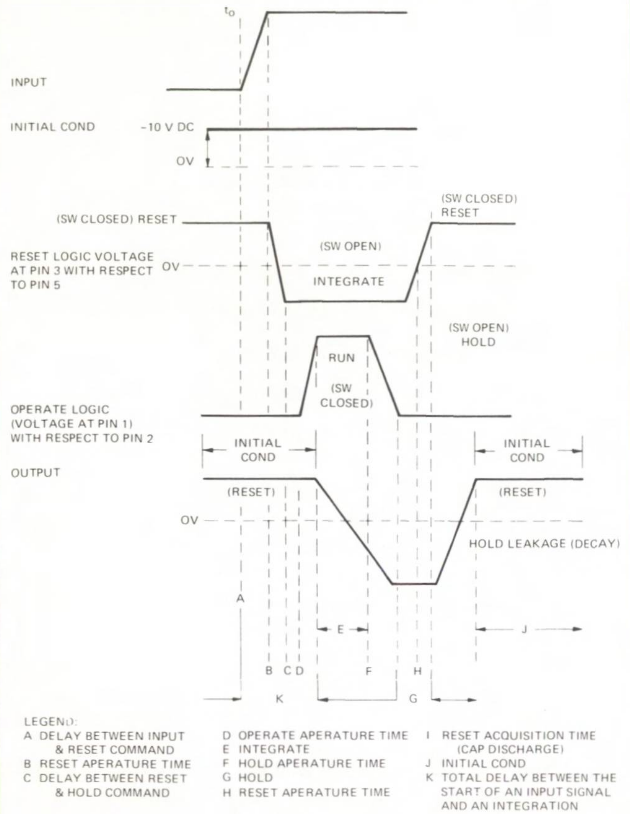
R_i = input resistance

C_f = integrating capacitance

E_{ic} = arbitrary initial value at $+\leqslant 0$

$K = 1$: if $R_{ic} = 10$ k or $\frac{10\text{ k}, \pm 0.1\%}{R_{ic}}$

Model 4850 Three Mode Integrator Timing Diagram



TRACK-AND-HOLD

The Model 4850 is useful as a track-and-hold operator. In this mode, the output tracks the input signal or holds the output value for a particular time. Operation is controlled only by the polarity of the FET switch (pin 3).

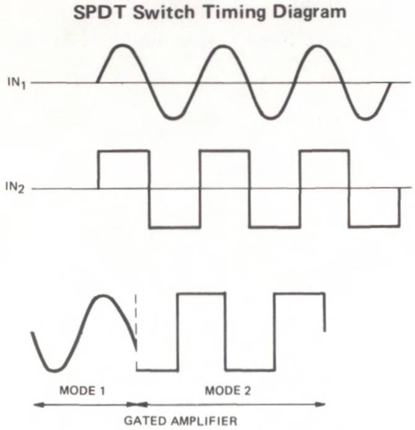
During the tracking operation, the output follows the inverse of the input and can be amplified by a constant, K, depending upon the value of the initial condition input resistance, R_{ic}, which is determined as follows:

$$R_{ic} = \frac{10\text{ k} \pm 0.1\%}{K}$$

ELECTRONIC SPDT SWITCH

When the Reset FET switch, internal to Model 4850, is closed it absorbs all of the input current from pin 6. It is possible, therefore, to switch between the two input signals at arbitrary gains and obtain a "chopped" output of the two signals by utilizing this switch as a control.

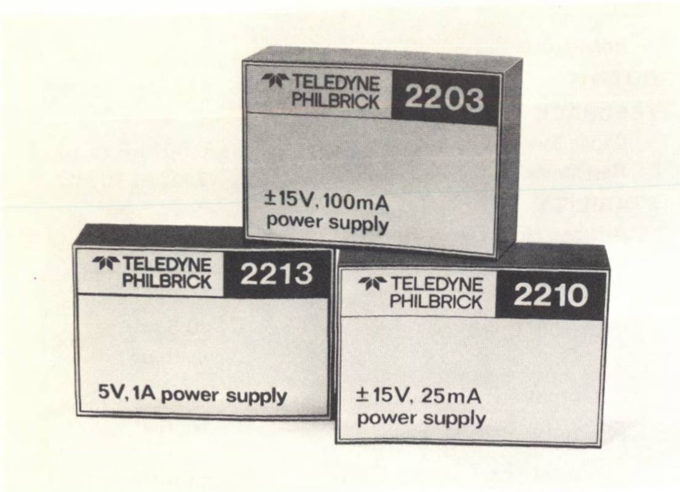
SPDT Switch Timing Diagram



ACCURACY	±0.1%
INPUT	
Voltage	±10 V
Impedance	2 kΩ to 10 MΩ
OUTPUT	±10 V @ ±20 mA
FEEDBACK	
Capacitance	0.001 μF to 10 μF
Resistance	2 kΩ to 10 MΩ
STABILITY	
Average Hold Decay Rate at +25 °C, max.	$\frac{\pm.06\text{ mV}}{\text{C (in } \mu\text{F)}}$ (max.)
at +60 °C, max.	$\frac{\pm 0.5\text{ mV}}{\text{C (in } \mu\text{F)}}$ (max.)
Output Switching Jump, max.	$\frac{\pm 0.05\text{ mV}}{\text{C (in } \mu\text{F)}}$ (max.)
Feedthrough	
Operate FET Switch Open	±1 mV
SWITCHING PERFORMANCE	
Aperture Time	800 nSec
Acquisition Time (Settling to 0.05%)	80 μSec
MODE CONTROL COMPARATORS	
Minimum Logic Level	±0.35 V
Maximum Logic Level	±5 V
Reference Level	±6 V
TEMPERATURE STABILITY	
Operate Mode	±35 μV/°C (max.)
Reset Mode	±3 mV/°C (max.)
TEMPERATURE RANGE	0 °C to +60 °C
POWER REQUIREMENT	±15 V @ ±70 mA
CASE STYLE	T-10
SOCKET	6024 ($4.00)

1. Specifications are typical at +25 °C, V_{CC} @ ±15 V, unless otherwise indicated.

POWER SUPPLIES



FEATURES

- Small Size (Encapsulated Modules)
- Short Circuit Protection
- Excellent Line and Load Regulation
- 25 mA to 1000 mA Output Current
- No RFI Generated or Transmitted
- Versatile and Trimmable (Models 2203/2204)
- Custom Modifications Available

Reliable power is the foundation of analog or logic systems. Teledyne Philbrick designs and manufactures a comprehensive line of Power Supplies for logic networks and circuit modules such as operational amplifiers, digital-to-analog and analog-to-digital converters, and nonlinear circuit modules.

	HIGH PERFORMANCE					LOW COST		
	2203	2204	2208	2209	2210	2211	2212	2215
OUTPUT								
Voltage (±1%)	±15 V	±15 V	±15 V	±15 V	±15 V	±15 V	±15 V	±15 V
Current, operating	±100 mA	±50 mA	±100 mA	±50 mA	±25 mA	±50 mA	±100 mA	±200 mA
Current, short circuit	±60 mA	±30 mA	±60 mA	±30 mA	±45 mA	±90 mA	±140 mA	±360 mA
REGULATION								
Line, max. (105-125 Vac)	±0.03%	±0.03%	±0.03%	±0.03%	±0.2%	±0.1%	±0.05%	±0.02%
Load, max (0-100%)	±0.03%	±0.015%	±0.03%	±0.015%	±0.2%	±0.1%	±0.1%	±0.05%
Temperature coefficient, max.	±0.01%/°C	±0.01%/°C	±0.01%/°C	±0.01%/°C	±0.02%/°C	±0.015%/°C	±0.015%/°C	±0.02%/°C
Warm-up drift	45 mV	35 mV	45 mV	35 mV	30 mV	35 mV	45 mV	45 mV
Ripple and noise, max.	1 mV rms	1 mV rms	1 mV rms	1 mV rms	1 mV rms	1 mV rms	1 mV rms	1 mV rms
Impedance @ 10 kHz	0.2 Ω	0.2 Ω	0.2 Ω	0.2 Ω	0.2 Ω	0.2 Ω	0.2 Ω	0.2 Ω
TEMPERATURE RANGE								
Operating (°C)	-25 to +85	-25 to +85	-25 to +85	-25 to +85	0 to +70	0 to +70	0 to +70	0 to +70
Storage (°C)	-35 to +125	-35 to +125	-35 to +125	-35 to +125	-25 to +85	-25 to +85	-25 to +85	-25 to +85
INPUT								
Voltage (±10%)	115/230 Vac	115/230 Vac	115 Vac	115 Vac	115 Vac	115 Vac	115 Vac	115 Vac
Isolation	50 MΩ	50 MΩ	50 MΩ	50 MΩ	50 MΩ	50 MΩ	50 MΩ	50 MΩ
Frequency (Hz)	50 to 400	50 to 400	50 to 400	50 to 400	50 to 400	50 to 400	50 to 400	50 to 400
Case Style (See page 63)	C1	C1	C3	C3	C4	C4	C3	C5
Mating Socket (See page 68)	6036	6036	6036	6036	6036	6036	6036	6036
Options*	––	––	21	21	21	21	21	221521

* Options Available

For 230 Vac, 50-400 Hz input, add the suffix "21" to the model number. No additional charge.

** (±2%)

All power supplies are complete and self-contained. No external transformers or filters are required for stable, accurate operation. This one unit construction is easier to use, and reduces component and assembly costs of the equipment being manufactured. For added mechanical strength the encapsulated supplies can be fastened to a P.C. Board or in optional mating sockets by supplied hold-down nut.

PROTECTION

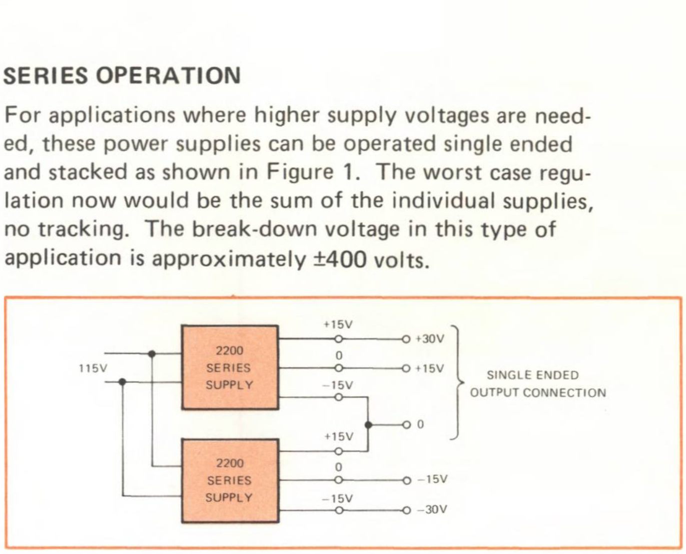
All Teledyne Philbrick power supplies are protected against overheating from direct short circuits to ground. The dual supplies will track each other so that a short on one output will automatically reduce the other output to prevent damage to the load circuitry.

LOW COST		MICROLOGIC		HI POWER
2216	**2217**	**2206**	**2213**	**2207**
±26 V	±120 V	+5 V	+5 V	±15 V
±45 mA	±40 mA	+500 mA	+1000 mA	±500 mA
±60 mA	±75 mA	+150 mA	+1.2 Amp	±150 mA
±0.05%	±0.01%	±0.1%	±0.05%	±0.02%
±0.05%	±0.01%	±0.15%	±0.1%	±0.05%
±0.02%/°C	±0.05%/°C	±0.01%/°C	±0.02%/°C	±0.03%/°C
35 mV	––	15 mV	25 mV	25 mV
1 mV rms	2 mV rms	2 mV p-p	1 mV rms	5 mV p-p
0.2 Ω	0.8 Ω	0.1 Ω	0.2 Ω	0.2 Ω
0 to +70	0 to +70	-25 to +85	-25 to +70	-20 to +50
-25 to +85	-25 to +85	-35 to +125	-55 to +85	-40 to +75
115 Vac	115 Vac	115/230 Vac	115 Vac	115 Vac
50 MΩ	50 MΩ	50 MΩ	50 MΩ	100 MΩ
50 to 400	50 to 400	50 to 400	50 to 400	50 to 400
C5	C6	C1	C5	C2
6036	6036	6036	6036	––
221621	221721	––	21	21

Characteristics typical at 25°C with nominal line voltage, unless otherwise indicated.

SERIES OPERATION

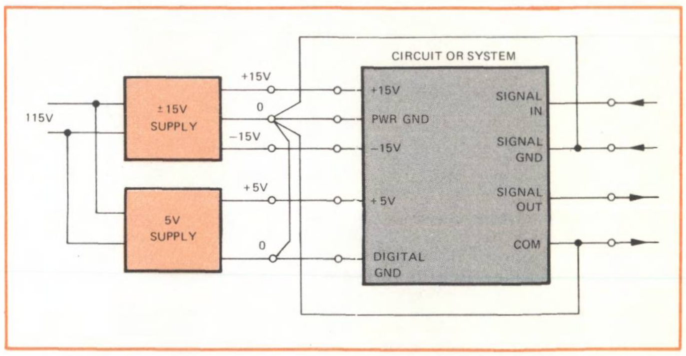
For applications where higher supply voltages are needed, these power supplies can be operated single ended and stacked as shown in Figure 1. The worst case regulation now would be the sum of the individual supplies, no tracking. The break-down voltage in this type of application is approximately ±400 volts.



GROUNDING PROCEDURES

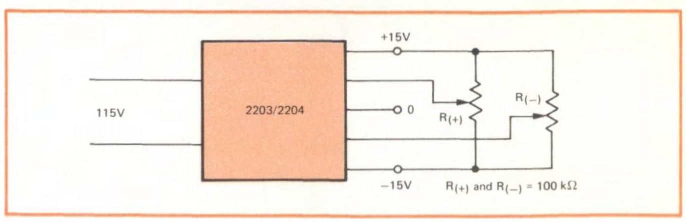
Power supply grounding is one of the most important factors in powering analog loads. Very often system design problems can be avoided or completely eliminated by following good grounding procedures.

We recommend that all ground points be tied together at a single point to minimize the noise and excessive ground currents caused by differences in ground potential. These connections should be as short as possible impedance.



TRIMMING

Models 2203 and 2204 have trim terminals which allow adjustment of the output voltage from ±14.5 to ±15.5 Vdc. The trimming hookup is given below.

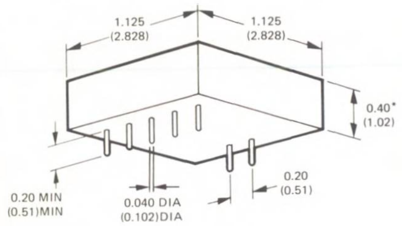


MECHANICAL SPECIFICATIONS

All dimensions in parentheses are expressed in centimeters.

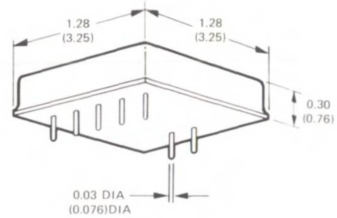
Unless otherwise specified, module pins are 0.04 (0.10) diameter and are spaced 0.20 (0.51) apart. Spacing between rows of pins is 0.80 (2.03).

A1 & A4
Socket NSK-20

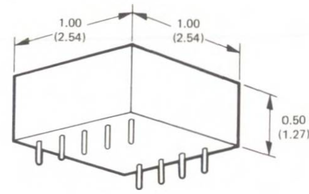


Case style A4 Height is 0.59 (1.40)

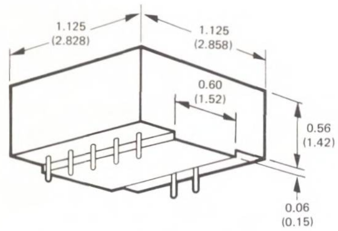
A5
Socket 6053



A6
Socket NSK-20

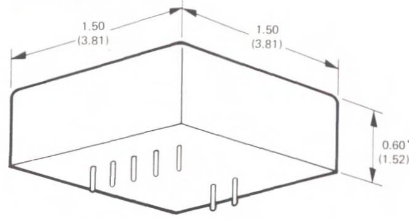


AS2
Socket NSK-20



Pin diameter for models PPT&H and PPL-4 is 0.03 (0.08)

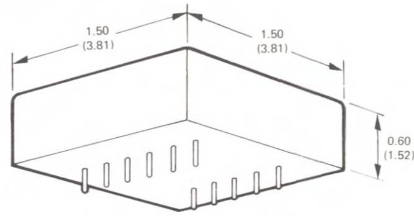
E5 & E5A
Socket NSK-20**



*Case style E5A height is 0.42 (1.05)

**Socket for Models 1029 and 1702 is 6123.

E5B
Socket 6129



MODEL	CASE	DIAGRAM	TRIM VALUE
1005	A1	A	50 kΩ RHST
1006	A1	B	1 kΩ POT
1008	A1	A	1 kΩ RHST
1017	A1	C	1 MΩ POT
1020/01-03	A1	A	**
1021	A1	A	2 kΩ RHST
1023/01	A1	A	**
1024	A1	A	10 kΩ RHST
1025	E5A	E	100 kΩ RHST
1026/01/02*	A1	A	10 kΩ RHST
1027/01	A4	A	1 kΩ RHST
1028	A6	A	50 kΩ RHST
1029/01	E5A	D	50 kΩ POT
1030	E5	B	100 kΩ POT
1034/01	E5A	A	50 kΩ RHST
1412	A5	D	50 kΩ POT
1701/01	E5	D	50 kΩ POT (Opt)
1702/01	E5	D	50 kΩ POT
1703/01	E5A	D	50 kΩ POT
4450	A1	D	50 kΩ POT
4452	E5	F	(2) 50 kΩ RHST
4454	E5B	G	---
4455	E5B	G	---
4456	E5B	G	---
4457	E5B	G	---
4353	E5	H	---
4354	E5	H	---
4357	A6	J	---
4358	A6	J	---
BQ-100	AS-2	K	---
PPL4-N/P	AS-2	K	---
PPT&H	AS-2	K	---

*Common Pin Not Used ** Metal Film Resistors Supplied

DIAGRAM A

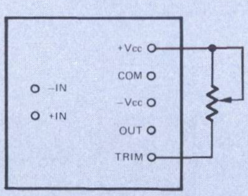


DIAGRAM B

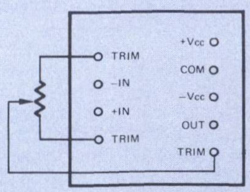


DIAGRAM C

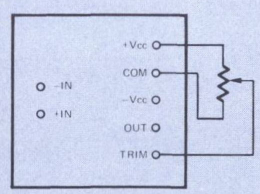
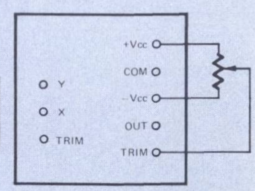


DIAGRAM D



FOR MODELS	1029 1702	1412 1701 1703
Pin Y is	−IN	−IN
Pin X is	+IN	HQ GND
TRIM Pin	NOT USED	

Common pin on model 1412 is Tied to Case.

DIAGRAM E

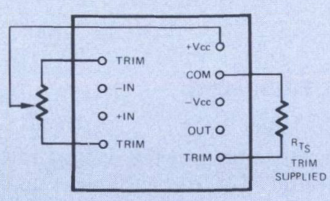


DIAGRAM F

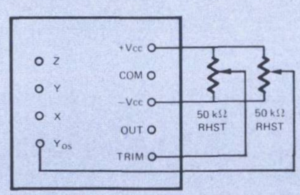
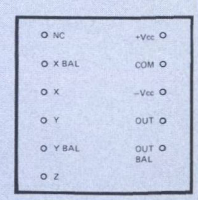


DIAGRAM G



ALL DIAGRAMS ARE BOTTOM VIEW

DIAGRAM H

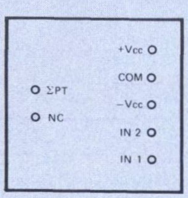


DIAGRAM J

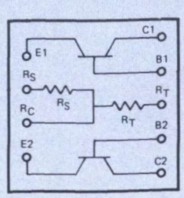
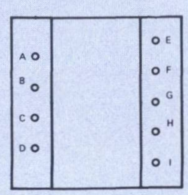
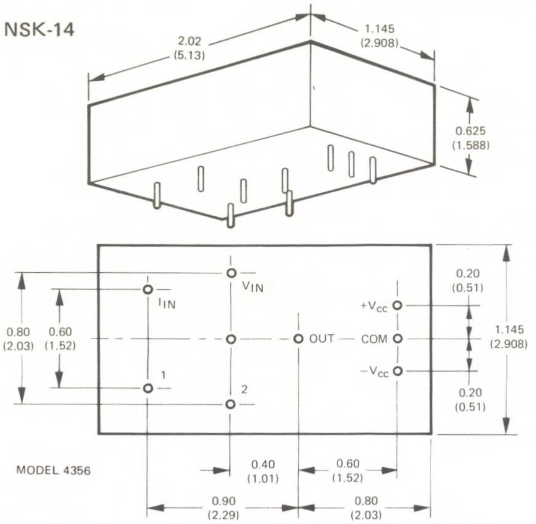


DIAGRAM K

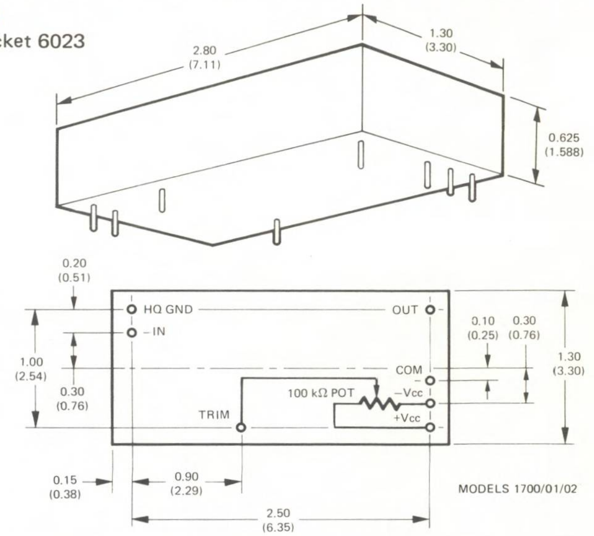


PIN	BQ-100	PPL4-N/P	PPT&H
A	–	3	SIG IN
B	NC	SUM PT	−IN
C	IN	SIG GRD	+IN
D	–	2	HQ GRD
E	+Vcc	+Vcc	+Vcc
F	COM	COM	COM
G	−Vcc	−Vcc	−Vcc
H	OUT	INPUT	OUT
I	NC	1	LOGIC

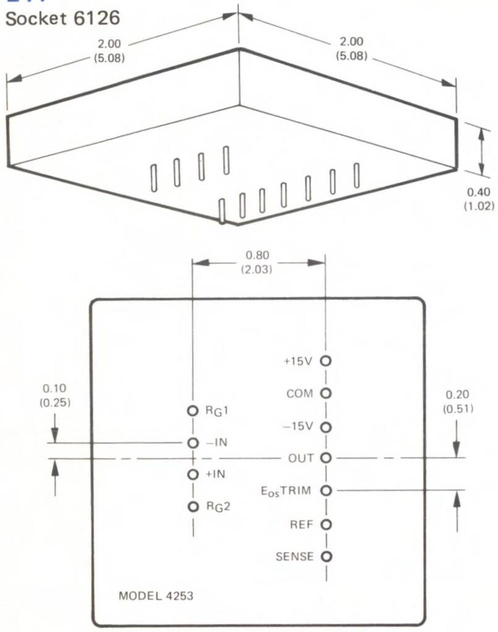
E1
Socket NSK-14



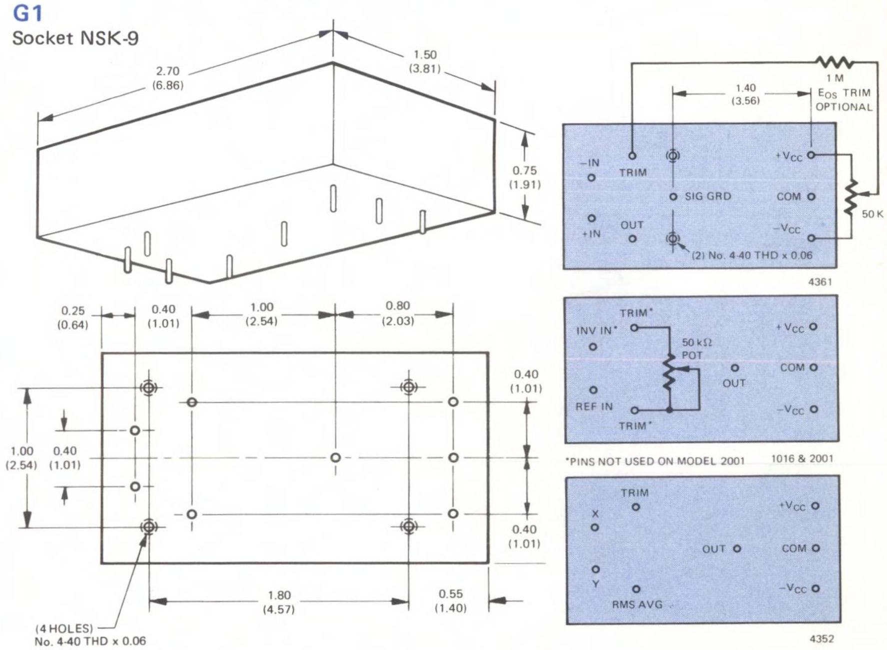
E4
Socket 6023



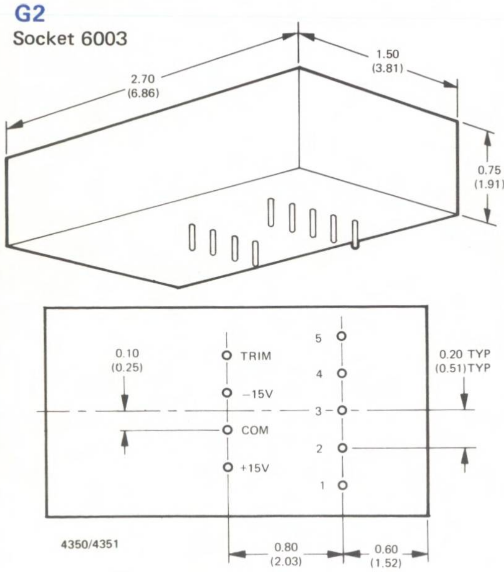
E11
Socket 6126



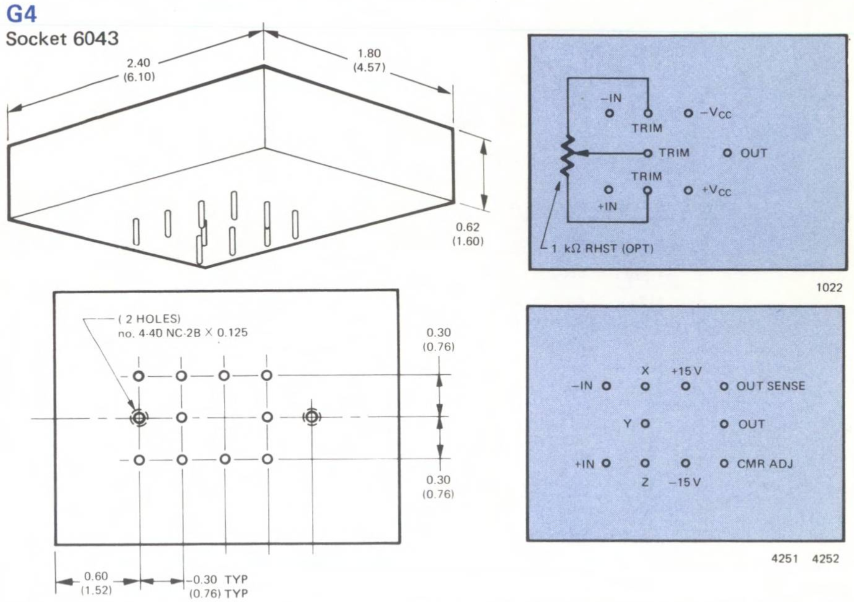
G1
Socket NSK-9



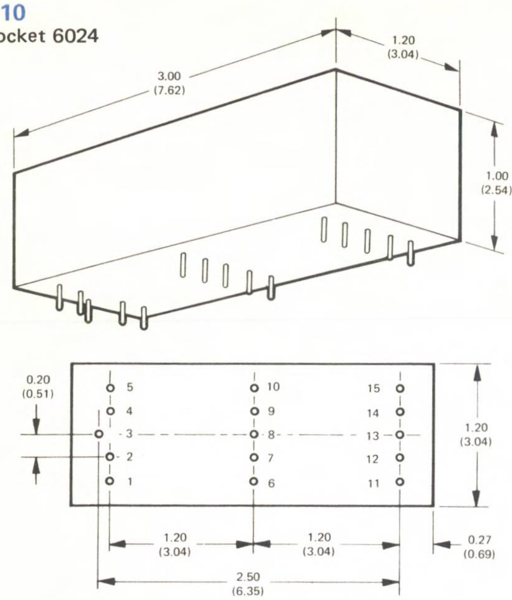
G2
Socket 6003



G4
Socket 6043

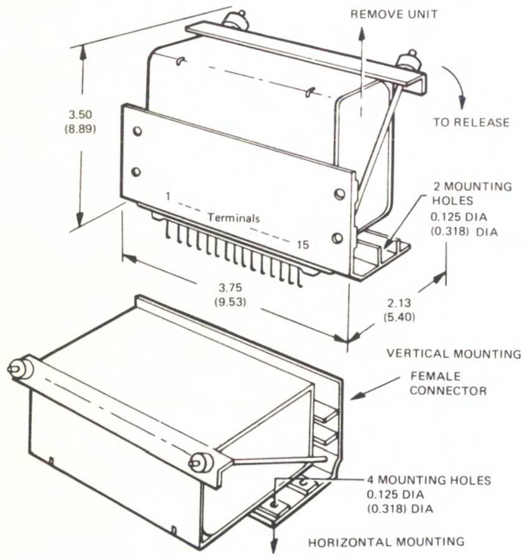


T10
Socket 6024



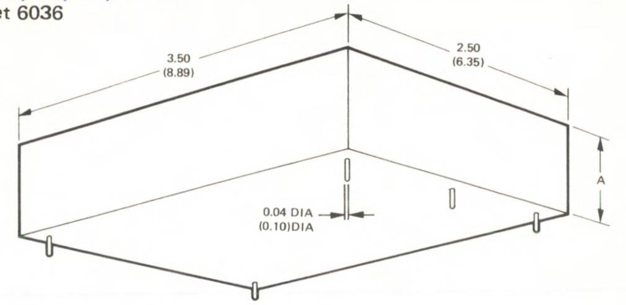
1. OPERATE INPUT
2. OPERATE REF INPUT
3. RESET INPUT
4. INITIAL CONDITION SUMMING POINT
5. RESET REFERENCE INPUT
6. SWITCHED SUMMING POINT
7. SUMMING POINT
8. SIGNAL GROUND
9. BOUND DETECTOR
10. TRIM A-2 (CURRENT AMP)
11. +15V
12. COMMON
13. −15 V
14. OUTPUT
15. TRIM A-1 (MAIN AMP)

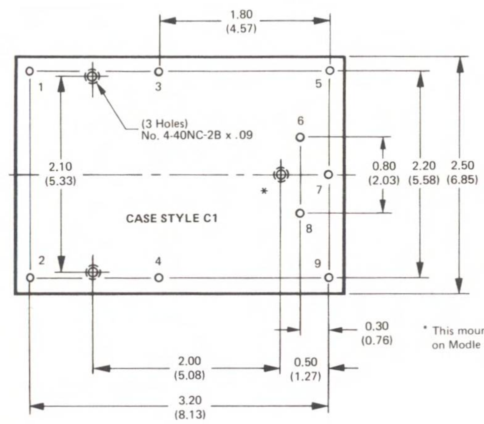
SP-MBSP



PIN	OSPB-100/10	SPFX-N/P	SP2A SP2AU
1	OUT	NC	OUT
2	−120 V	−15 V	−15 V
3	+120 V	+15 V	+15 V
4	KEY	NC	COM
5	INV. IN	NC	GUARD
6	NC	KEY	+IN
7	INPUT	ΣPT 1	−IN
8	COM	COM	COM
9	NC	IN	KEY
10	KEY	ΣPT 2	NC
11	−BOOST R	NC	COM
12	−BOOST R	NC	NC
13	+BOOST R	NC	NC
14	GROUND	NC	CASE
15	GROUND	CASE	CASE

C1, C3, C4, C5, & C6
Socket 6036

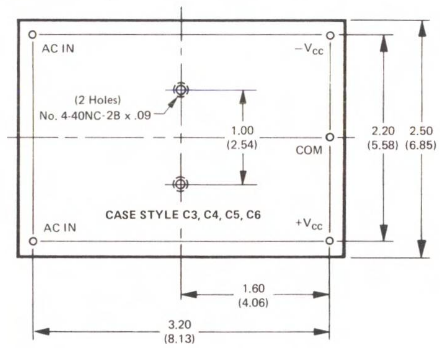




MODELS 2203, 2204, & 2206
PIN DESIGNATIONS

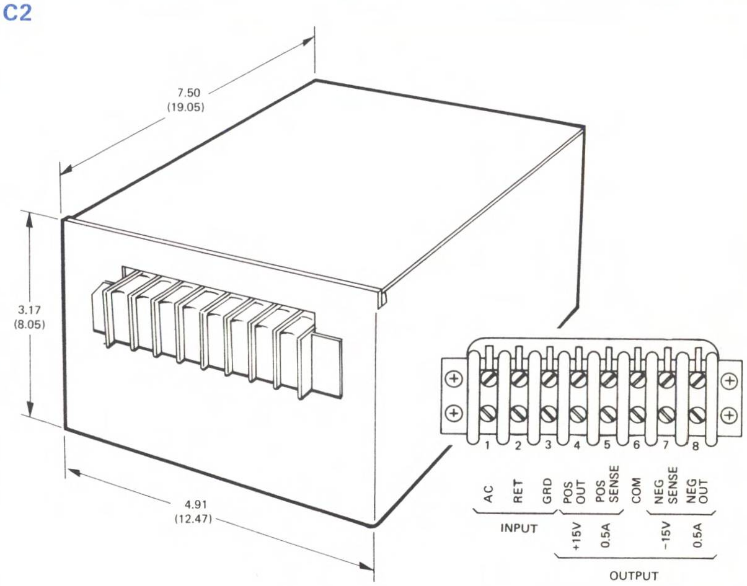
Pin	2203 2204	2206
1	AC	AC
2	AC	AC
3	AC	AC
4	AC	AC
5	$-V_c$	N.C.
6	TRIM	NO PIN
7	COM	COM
8	TRIM	NO PIN
9	$+V_c$	$+V_c$

* This mounting hole is not included on Modle 2206.

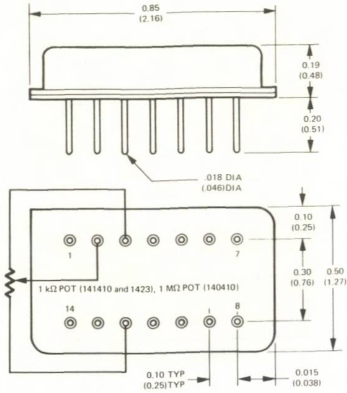


CASE	HEIGHT A
C1	1.00
C3	1.00
C4	0.88
C5	1.25
C6	2.00

C2



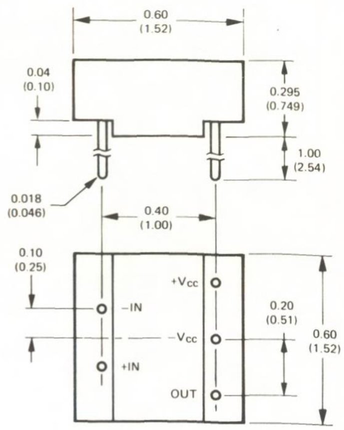
S4



PIN	140410 141410 1423	3420*	PIN	140410 141410 1423	3420*
1	NC	P	8	COM	G
2	TRIM	A	9	NC	H
3	TRIM	B	10	OUT	J
4	−IN	C	11	+Vcc	K
5	+IN	D	12	TRIM	L
6	−Vcc	E	13	NC	M
7	NC	F	14	NC	N

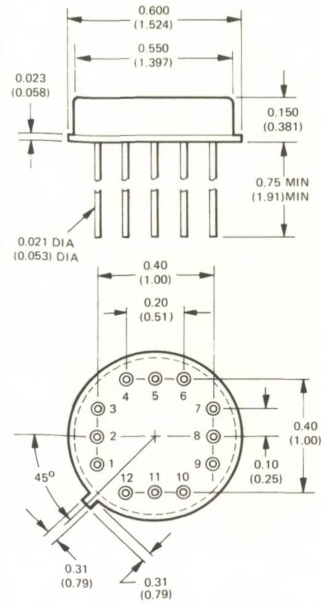
*Pin designations correspond to schematic diagram page 40.

T1
Socket 6035



MODEL 1428

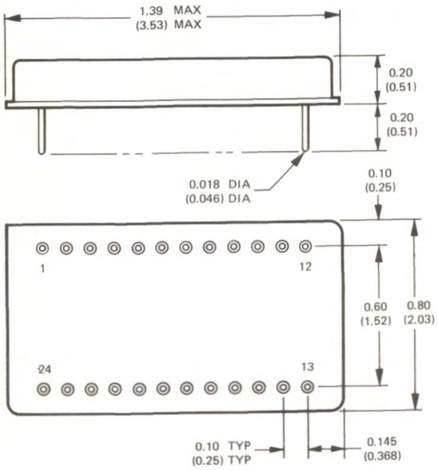
TO-8
Socket US-Q



PIN	1402/02	1427/01
1	TRIM	+IN
2	TRIM	−IN
3	TRIM	NC
4	+IN	+15 V
5	$-V_{CC}$	NC
6	NC	−15
7	NC	CASE
8	OUT	OUT
9	NC	NC
10	CASE	NC
11	$+V_{CC}$	NC
12	−IN	NC

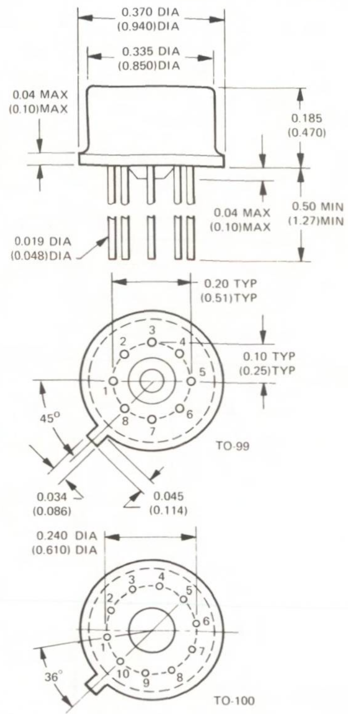
SERIES 1402 REQUIRES A 1 kΩ POT ACROSS PINS 1 AND 3 WITH THE ARM FROM PIN 2.

S5



PIN NO.	4050/4052/4054 4051/4053/4055		PIN NO.		
1	Bit 12 LSB	Ground on 8 &10 Bit models	13	Ref In	
2	Bit 11		14	Ref Out	
3	Bit 10	Ground on 8-bit models	15	Mode	
4	Bit 9		16	Sum Bus Out (Iout)	
5	Bit 8		17	Gain Resistor	
6	Bit 7		18	Gain Resistor	
7	Bit 6		19	Analog Voltage Out	NC on 4050 4052/4054
8	Bit 5		20	Eos Trim	
9	Bit 4		21	+15 V	
10	Bit 3		22	Common	
11	Bit 2		23	−15 V	
12	Bit 1 MSB		24	High Quality Ground	

TO-99 & TO-100



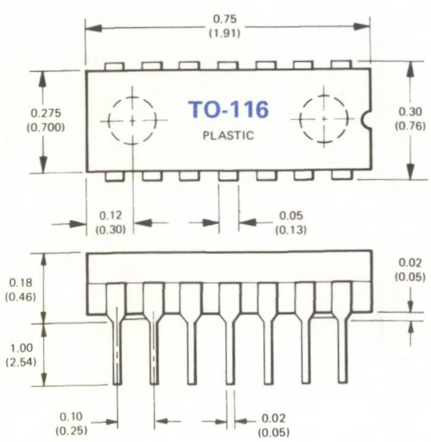
PIN	SERIES 1321/1322	SERIES 1323	SERIES 1339	SERIES 1319/1421/1422 1424/1425/1426/1429
1	OFFSET ADJUST	OFFSET ADJUST	INPUT LAG	OFFSET ADJUST
2	−IN	−IN	−IN	−IN
3	+IN	+IN	+IN	+IN
4	−Vcc	−Vcc	−Vcc	−Vcc
5	OFFSET ADJUST	NC	OUTPUT LAG	OFFSET ADJUST
6	OUTPUT	OUTPUT	OUTPUT	OUTPUT
7	+Vcc	+Vcc	+Vcc	+Vcc
8	BANDWIDTH CONTROL	OFFSET ADJUST	INPUT LAG	BANDWIDTH* CONTROL

*PIN 8 IS GUARD ON SERIES 1429.

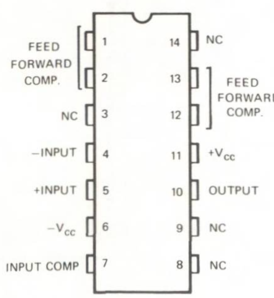
PIN	1317	1324/132401
1	OFFSET TRIM	FEED FORWARD COMP
2	−IN	FEED FORWARD COMP
3	OFFSET TRIM	−IN
4	+IN	+IN
5	−Vcc*	−Vcc
6	INPUT DAMPER	OUTPUT
7	INPUT DAMPER	COMPENSATION
8	OUTPUT DAMPER	+Vcc
9	OUTPUT	FEED FORWARD COMP
10	+Vcc	FEED FORWARD COMP

*PIN 5 IS INTERNALLY CONNECTED TO CASE.

TO-116 PLASTIC

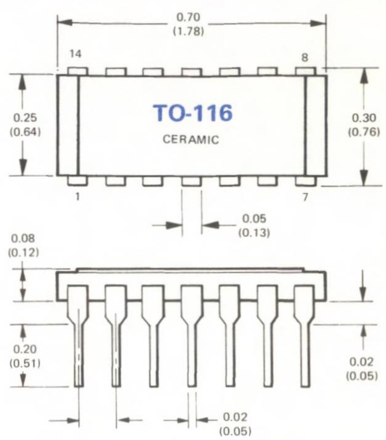


SERIES 132410/11/12



TOP VIEW

TO-116 CERAMIC

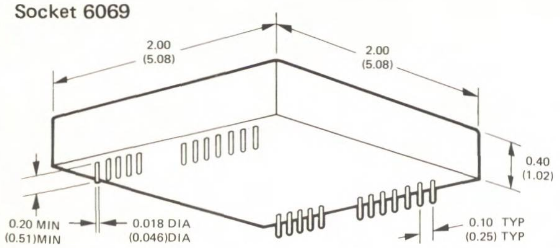


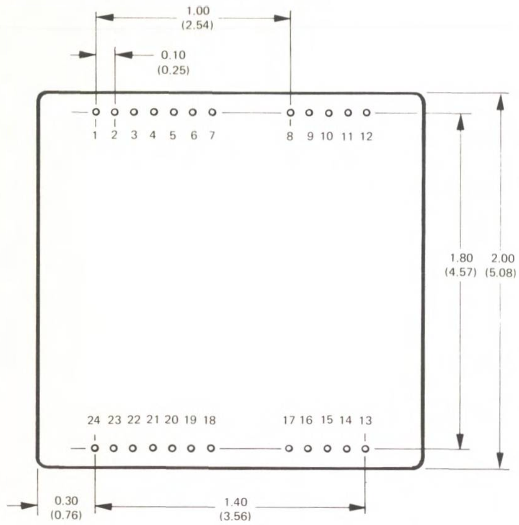
PIN	SERIES 132310/11/12
1	NC
2	OFFSET ADJUST
3	NC (GUARD)**
4	−IN
5	+IN
6	NC (GUARD)**
7	−Vcc*
8	NC
9	NC
10	OUTPUT
11	+Vcc
12	OFFSET ADJUST
13	NC
14	NC

*NOT STANDARD 741 CONFIGURATION

**TO MINIMIZE LEAKAGE CURRENT BETWEEN PINS, IT IS RECOMMENDED THAT PINS 3 & 6 BE GROUNDED

E6
Socket 6069

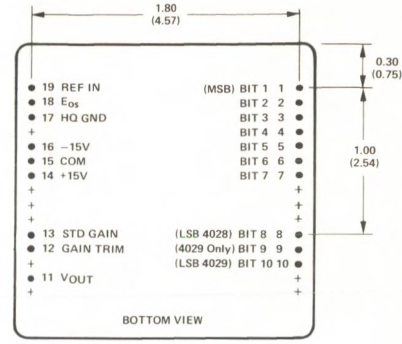




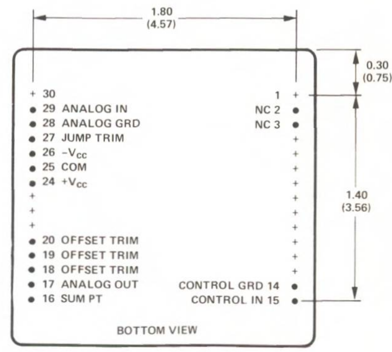
PIN	4004 4005 4024 4025	4008 4009 4026 4027	4010 4011 4022 4023	4020 4021
1			BIT 1	
2			BIT 2	
3			BIT 3	
4			BIT 4	
5			BIT 5	
6			BIT 6	
7			BIT 7	
8			BIT 8	
9			BIT 9	NOT USED
10			BIT 10	
11		BIT 11	NOT USED	
12		BIT 12	NOT USED	
13			I_{OUT}	
14			V_{OUT}	
15			NOT USED	
16	MODE	NOT USED	MODE	
17			REF OUT	
18			+15 VDC	
19			GROUND	
20			−15 VDC	
21			NOT USED	
22			+REF IN	
23			−REF IN	
24			EXT REF	

NOTES ON D–A CONVERTERS

1. UNIPOLAR MODE–CONNECT PIN 16 TO GROUND PIN 19
2. BIPOLAR MODE–CONNECT PIN 13 TO 16
3. PINS 13 AND 16 USED IN CURRENT CONVERTER ONLY.
4. PIN 14 USED IN VOLTAGE CONVERTER ONLY.
5. TO INSURE STABLE OPERATION, POWER SUPPLY BYPASSING WITH 0.01 μF DISC CAPACITOR IS RECOMMENDED.
6. BECAUSE OF THE HIGH SPEED BUFFER INPUTS IN THE DAC'S IT IS RECOMMENDED THAT ANY DIRECT GROUNDING OF DIGITAL INPUTS BE DONE THROUGH 100Ω RESISTORS TO PREVENT OSCILLATIONS. HOWEVER, THIS IS NOT NECESSARY IF THE INPUTS ARE DRIVEN DIRECTLY FROM A DTL OR TTL SOURCE.

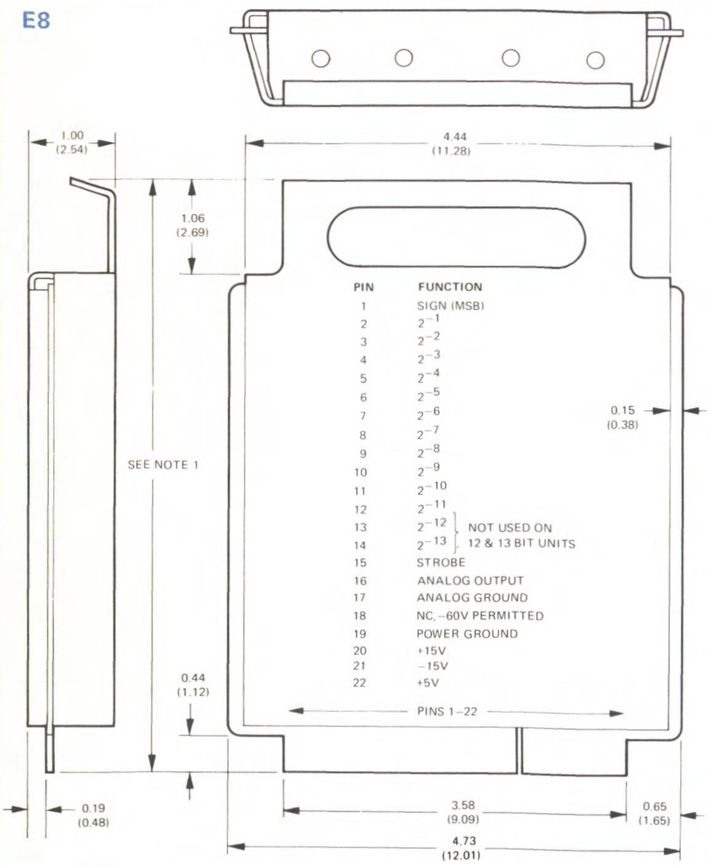


MODELS 4028 AND 4029



MODEL 4853

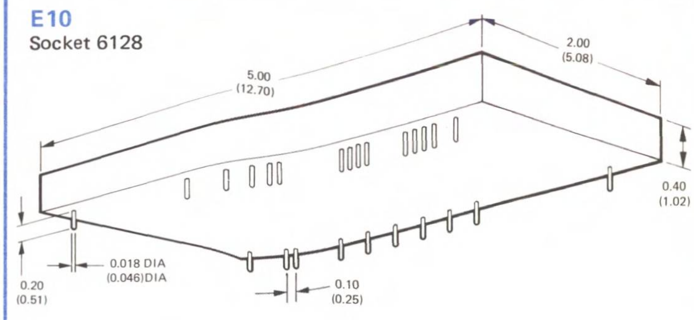
E8

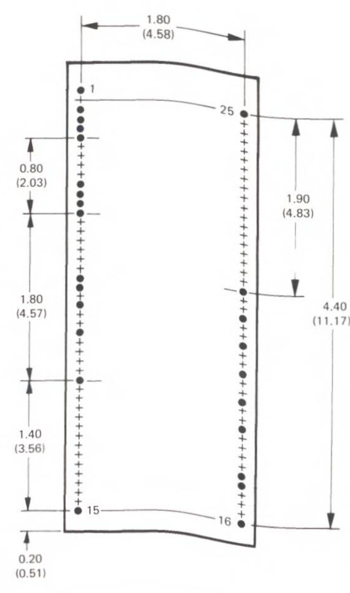


PIN	FUNCTION
1	SIGN (MSB)
2	2^{-1}
3	2^{-2}
4	2^{-3}
5	2^{-4}
6	2^{-5}
7	2^{-6}
8	2^{-7}
9	2^{-8}
10	2^{-9}
11	2^{-10}
12	2^{-11}
13	2^{-12} } NOT USED ON
14	2^{-13} } 12 & 13 BIT UNITS
15	STROBE
16	ANALOG OUTPUT
17	ANALOG GROUND
18	NC, −60V PERMITTED
19	POWER GROUND
20	+15V
21	−15V
22	+5V

NOTES:
1. HEIGHT FOR MODEL 4002 IS **6.31 (16.03)**. HEIGHT FOR MODELS 4015, 4017 is **8.13 (20.64)**
2. KEY SLOT (0.062) IS LOCATED BETWEEN PINS 16 AND 17.
3. DISTANCE BETWEEN FINGER CENTERS IS 0.156.
4. MATING CONNECTOR IS 22 PIN CINCH 250-22-30-170 OR EQUIVALENT (SUPPLIED)

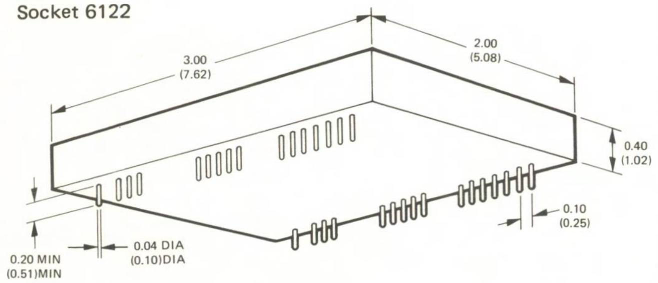
E10
Socket 6128

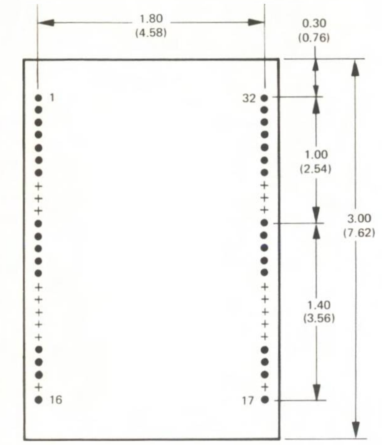




PIN	4014/4016
1	BIT 13 (4016 ONLY)
2	BIT 12
3	BIT 11
4	BIT 10
5	BIT 9
6	BIT 8
7	BIT 7
8	BIT 6
9	BIT 5
10	BIT 4
11	BIT 3
12	BIT 2
13	BIT 1
14	DIG GND
15	NC
16	+REF
17	−REF IN
18	REF OUT
19	DAC OUT
20	OFFSET
21	BINARY
22	−15 V
23	ANALOG GND
24	+15 V
25	NC

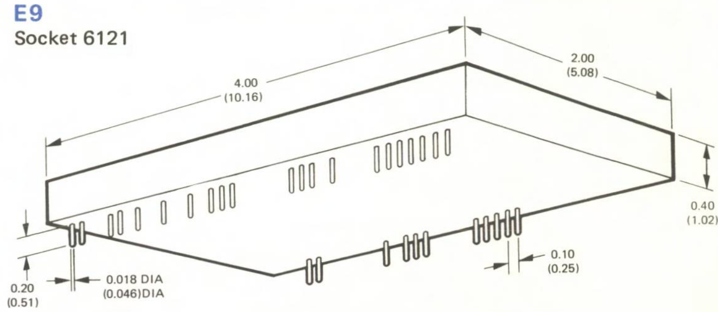
E7
Socket 6122

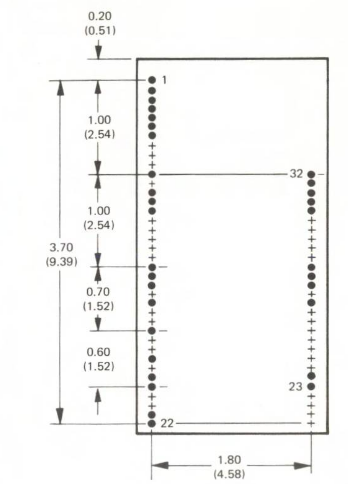




PIN	4109/01 4111/01	4110
1	NO PIN	E_{IN}
2	NO PIN	OFFSET
3	NO PIN	NO PIN
4	MSB	−15 V
5	RESET	COM
6	RECYCLE	+15
7	OFFSET	CLOCK A
8	NO PIN	DIGITAL GND
9	STATUS	TRACK LOW
10	OVERRANGE	TRACK HIGH
11	+5 V	CLOCK B
12	DIGITAL GND	INHIBIT
13	ANALOG GND	NO PIN
14	INPUT	NO PIN
15	NO PIN	NO PIN
16	NO PIN	NO PIN
17	−15 V	NO PIN
18	NO PIN	NO PIN
19	+15 V	NO PIN
20	NO PIN	NO PIN
21	BIT 1	+5 V
22	BIT 2	RESET
23	BIT 3	HIGH LIMIT
24	BIT 4	LOW LIMIT
25	BIT 5	BIT 8
26	BIT 6	BIT 7
27	BIT 7	BIT 6
28	BIT 8	BIT 5
29	BIT 9	BIT 4
30	BIT 10	BIT 3
31	BIT 11	BIT 2
32	BIT 12	BIT 1

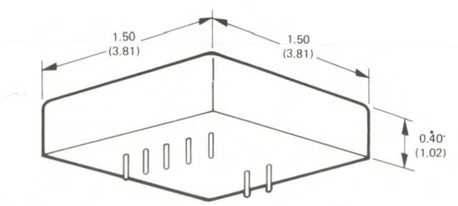
E9
Socket 6121

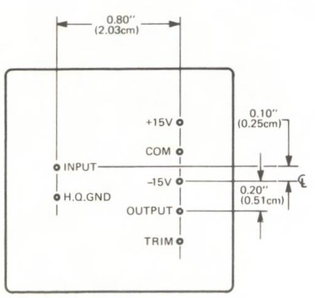




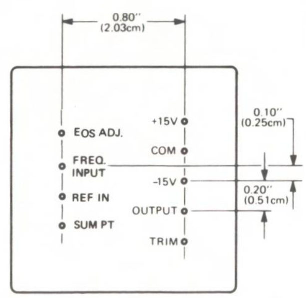
PIN	4103/4104/4105 4106/4107/4108 4112/4113	
1	BIT 12	12-bit models ONLY
2	BIT 11	
3	BIT 10	12 & 10-bit models ONLY
4	BIT 9	
5	BIT 8	
6	BIT 7	
7	BIT 6	
8	BIT 5	
9	BIT 4	
10	BIT 3	
11	BIT 2	
12	BIT 1	
13	$\overline{\text{MSB}}$	
14	EXT REF	
15	−REF IN	
16	E_{IN}	
17	−15 V	
18	+15 V	
19	SIG GND	
20	MODE	
21	REF OUT	
22	OFFSET	
23	SUM PT – No pin on Models 4106 4107 4108	
24	+5 V	
25	POWER GND	
26	INHIBIT	
27	SERIAL OUT	
28	CLOCK IN	
29	RESET	
30	CLOCK OUT	
31	$\overline{\text{STATUS}}$	
32	STATUS No pin on Models 4112 4113	

E5A
Socket NSK-20



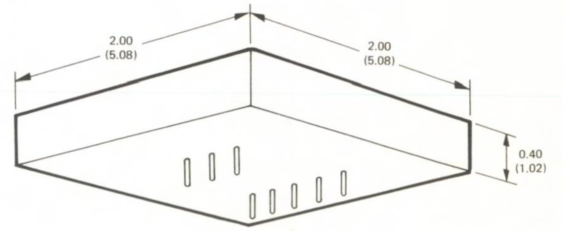


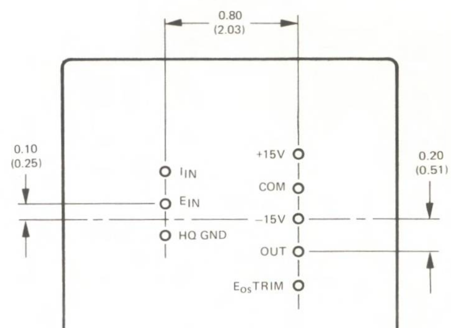
MODELS 4701 and 4703



MODELS 4702 and 4704

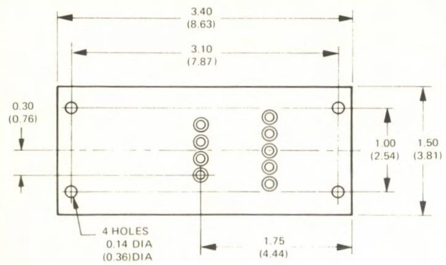
E12
Socket NSK-20





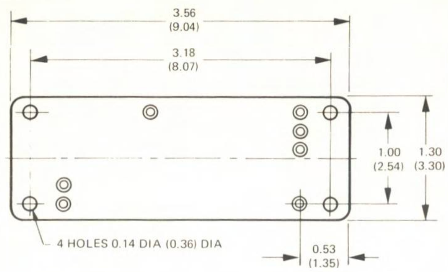
MODEL 4705

6003



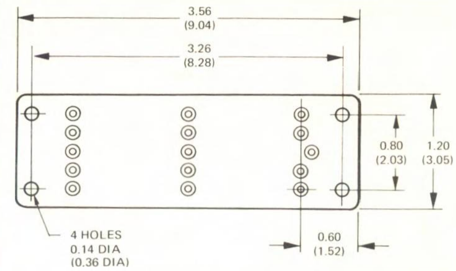
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

6023



BOARD THICKNESS: 0.09 (0.23) ALUMINUM
OVERALL HEIGHT: 0.50 (1.27)

6024



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OVERALL HEIGHT: 0.50 (1.27)

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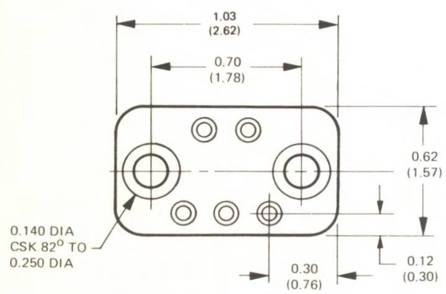

BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

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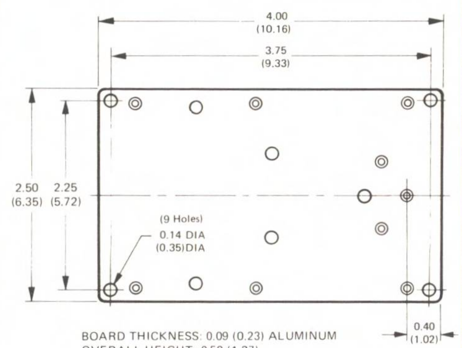
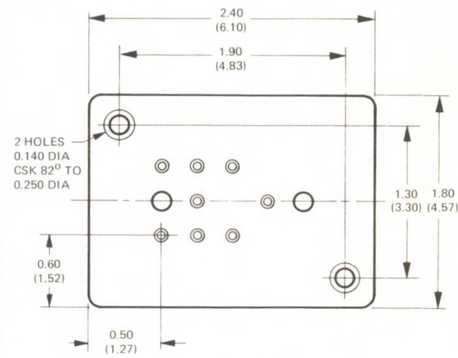


BOARD THICKNESS: 0.09 (0.23) ALUMINUM
OVERALL HEIGHT: 0.50 (1.27)

6043



BOARD THICKNESS: 0.09 (0.23) ALUMINUM
OVERALL HEIGHT: 0.50 (1.27)

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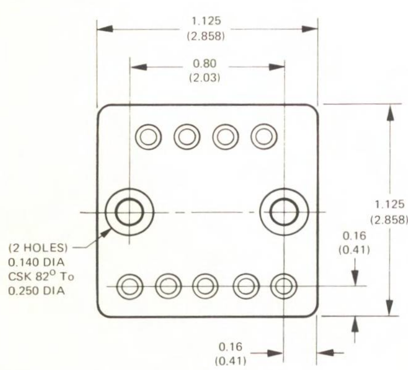

BOARD THICKNESS: 0.09 (0.23) ALUMINUM
OVERALL HEIGHT: 0.50 (1.27)

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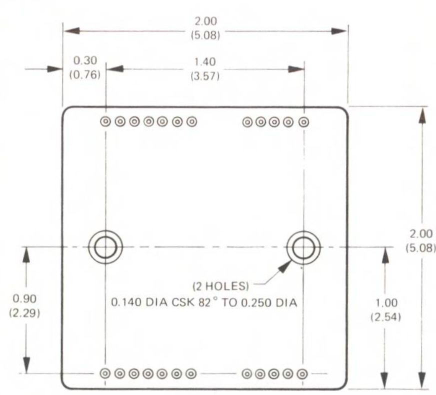
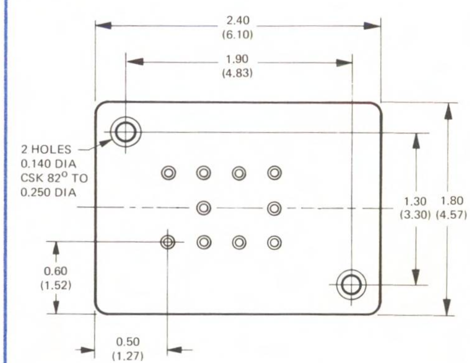


BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.50 (1.27)

6118



BOARD THICKNESS: 0.09 (0.23) ALUMINUM
OVERALL HEIGHT: 0.50 (1.27)

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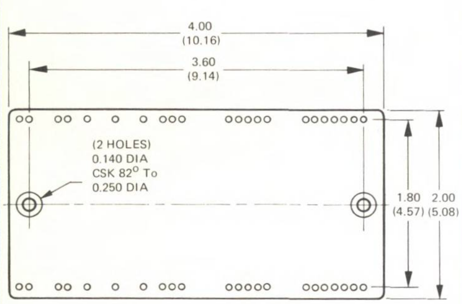
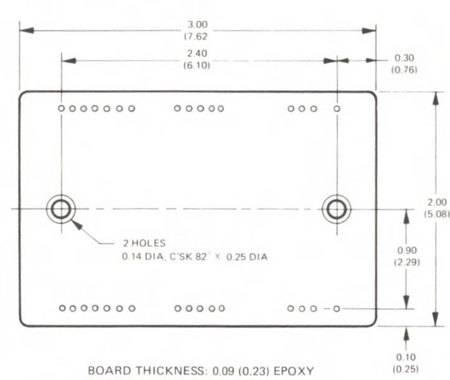


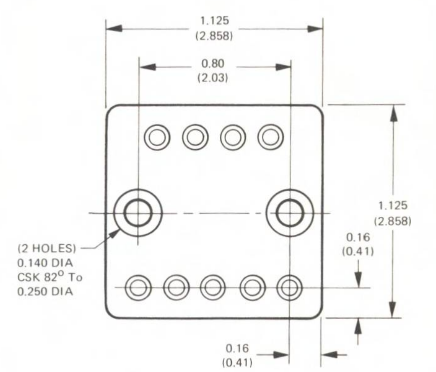
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

6122



BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

6123



BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

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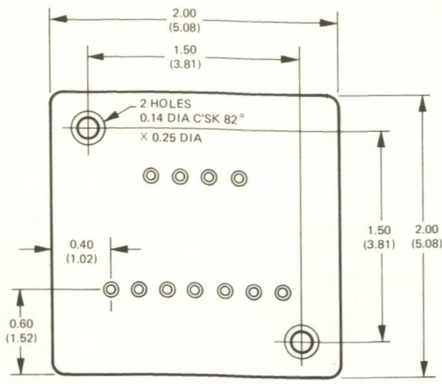
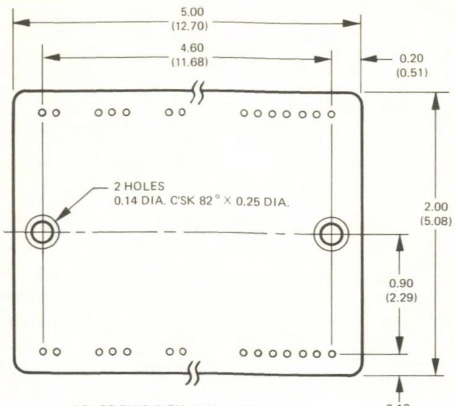


BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.50 (1.27)

6128



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OVERALL HEIGHT: 0.50 (1.27)

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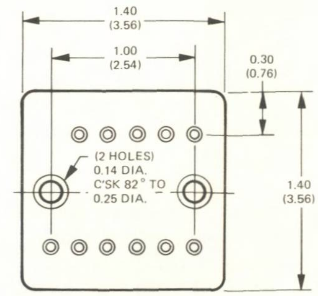
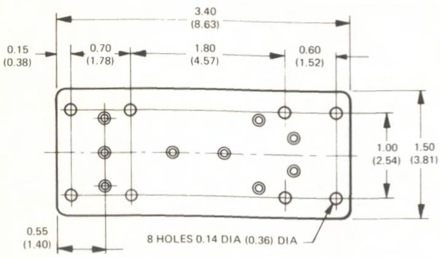


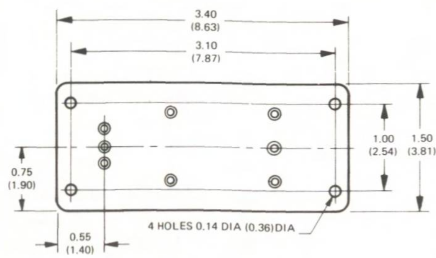
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.50 (1.27)

NSK-9



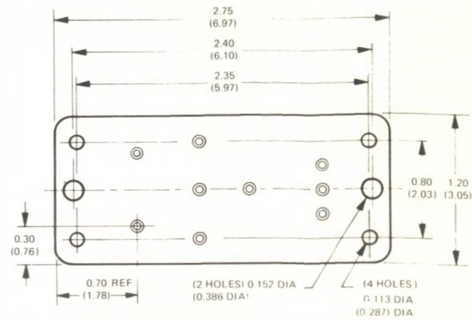
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

NSK-13



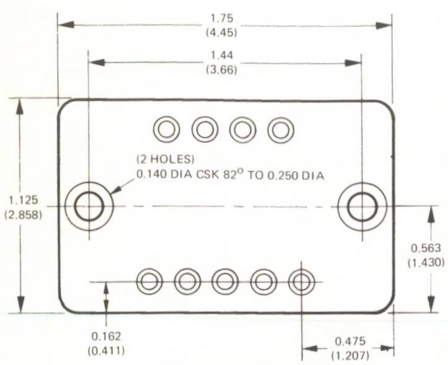
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

NSK-14



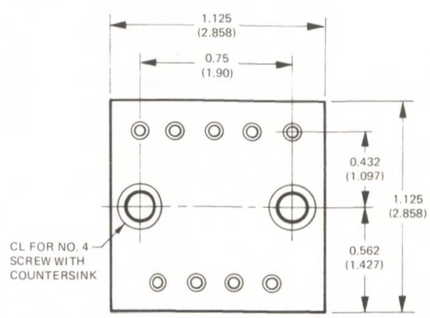
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

NSK-20



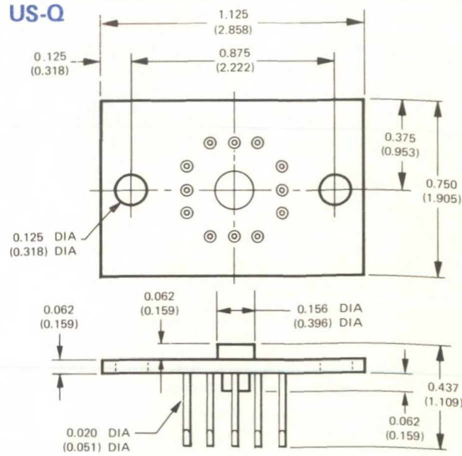
BOARD THICKNESS: 0.09 (0.23) EPOXY
OVERALL HEIGHT: 0.68 (1.73)

US-PP



BOARD THICKNESS: 0.125 (0.318) EPOXY
OVERALL HEIGHT: 0.43 (1.08)

US-Q



Standard Products still available, not recommended for New Designs.

Model	Description	Model	Description	Model	Description
1003	FET, High CMRR, Low Drift	1408	FET, Economy, Epoxy	Q25AH	FET, High Reliability, TO-8
100301	FET, High CMRR, Low Drift	140801	FET, Economy, Epoxy	Q200	Micropower
1009	FET, General Purpose	140802	FET, Economy, Epoxy	QFT-2	FET, General Purpose
100901	FET, General Purpose	140810	FET, Economy, TO-8	QFT-2A	FET, General Purpose
100902	FET, General Purpose	140811	FET, Economy, TO-8	QFT-2B	FET, General Purpose
1011	FET, Fast Differential	140812	FET, Economy, TO-8	SA-1	High Performance
101101	FET, Fast Differential	P2A	Premium, Parametric	SA-2	High Performance
101102	FET, Fast Differential	P65AU	General Purpose	SA-3A	High Performance
1018	Low Drift, Differential	P85AU	High Performance	SP2A	Premium Parametric
101801	Low Drift, Differential	PP45	Fast Inverting	SP2AU	Economy Parametric
101802	Low Drift, Differential	PP45U	Fast Inverting	SQ-3	High Input Impedance
101803	Low Drift, Differential	PP65A	High Reliability, General Purpose	SQ-10A	General Purpose
101804	Low Drift, Differential	PP65AU	General Purpose		
1019	FET, Fast Differential	PP85AU	High Performance		

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